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3D Interconnects with IC’s Stack Global Electrical Context Consideration

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4.1 Introduction

Three-dimensional (3D) Si integration seems like the right way to compete with Moore’s law (more than Moore versus more Moore). However, it is still a long way to go.
In 2010, the question was: Why 3D? Today, the questions are: When to use 3D and how to use 3D? The 3D chip stacking is known to overcome conventional 2D-IC issues, using in-depth contacts or through-silicon for signal transmission.

Mixed Signal ICs design has become key for systems-on-chip (SoCs) VLSIs. Functional analog blocks such as LNA, filters, and AD/DA converters, are placed on a die with high speed digital processing elements composed of a few million digital gates. Parasitic phenomenon, commonly called crosstalk, occurs between the noisy digital and the sensitive analog part of the device. Due to many parasitic coupling mechanisms, there is a distinct possibility that the transient regimes in the digital circuitry of this kind of device will corrupt low-level analog signals and seriously compromise the achievable performance [1]. One of the main coupling phenomena is the substrate coupling. The chip substrate acts as a collector, integrator, and distributor of coupled noise on chip. Many developments describe methods to simulate this perturbing kind of noise [2–4]. However, the majority of the models presented only considers the package bonding, whereas many different parts of the supply lines are important in substrate noise generation [5,6]: PCB, package, padring, on chip metal lines, and other parasitic elements of supply lines.

Nowadays, micro/nanotechnology and the development of semiconductor technology enable designers to integrate multiple systems into a single chip, not only in two-dimensional (2D) (planar), but also in 3D (in the bulk). This design technology reduces cost, while improving performance and makes the possibility of a system to be on chip [1–4].

The kind of silicon substrate in which 3D interconnections are processed is an important parameter and has a strong impact on 3D interconnection electrical behavior. Electrical modeling methods are dependent on the substrate type of the application. Two different kinds of P silicon substrates are typically used in CMOS/BiCMOS processes: uniform lightly doped substrate (>1Ω.cm) and heavily doped substrate (<1Ω.cm) with lightly thinned doped (>1Ω.cm) epitaxial layer. Other semiconductor substrates are used in micro/nano technologies and could embed 3D interconnections (SOI technologies, MEMS technologies, sensor technologies).

Advancements in the field of V(U)LSI have led to more compact ICs having higher clock frequencies and lower power consumptions. The paradigms of these integrated technologies are SoCs and Systems-in-Package (SiPs). Now, these conventional 2D planar technologies face several strategic challenges: physical limits, processing complexity, fabrication costs, and so on. Consequently, technological approaches other than scaling are investigated to continue following or get over Moore’s Law. Currently, 3D integrated systems can be obtained by stacking vertically 2D integrated circuits using mature, controlled micro and nano technologies. The electrical connections are ensured by new pre- or post-processed metallic structures (Figure 4.1): redistribution layers (RDL), which distribute power and high speed signals on die top or backside surfaces; copper pillars and mostly through-silicon via (TSV) are keys enabling technology for 3D integration, by propagating signals through the silicon layers.
Chips can also be stacked vertically using wire-bonding and flip-chip techniques. However, the flip-chip technique solely provides an interconnection between two chips; whereas, wire-bonding only enables the connection of chip input/output pads located at their perimeter. Moreover, wire-bonding presents disadvantages in terms of surface and propagation delays depending on the application frequency clock and the wire-bond lengths. Finally, solder balls are put on the 3D systems bottom layers backsides to ensure connection with their environment. Compared with 2D classical schemes, 3D integration potential benefits are numerous: performance improvement, flexible heterogeneous system combinations (logic CMOS, RF analog function, memories, and sensors), significantly shortened interconnect line networks that decrease interconnect line delays and power consumption (which become significant obstacles in 2D VLSI systems relative to delays in transistor switching), smaller form factors, and reduced fabrication costs [1,2].

Many challenges are encountered with 3D integration due to its status as an emerging technology, notably in properly characterizing and electrically modeling the 3D interconnects. Few present-day CAD tools can design 3D architectures. Many works have been mainly dedicated to advanced TSV electrical modeling.

Different types of via play a central role in realizing high-density integrated 3D systems. This enables a large variation in shape, dimension (radius, length), dielectric thickness, and filling material. The difficulty in TSV modeling is that the overall 3D interconnection electrical context must be considered. For example, current paths must be modeled if the environment comprises top/back redistribution metal lines. As with local metal layer interconnect line structures, the 3D interconnect global environment requires the modeling of the substrate coupling effects which can no longer be neglected at high frequency. Several substrate extraction techniques have been proposed in the literature but most of them cannot be employed for SoCs with realistic dimensions or are only suitable for a particular type of structure or technology process [7,8].

**FIGURE 4.1**
Schematic diagram showing the main mechanisms of substrate noise generated by a CMOS inverter.
4.2 Substrate Noise Generators and Propagation

In this section, we describe the different injection mechanisms in a digital device. Most CMOS logic elements can be reduced into simple CMOS inverters. Figure 4.1 shows a CMOS inverter and its different substrate noise sources.

The main substrate noise source is due to the power and ground bounces that are transmitted into the substrate through its biasing contacts [6]. In a CMOS inverter, the NMOS source transmits the ground bounce and the PMOS source transmits the power fluctuations. The power and ground bounces are generated by large transient-current spikes pulled by the simultaneous switching of multiple digital gates. Those spikes and the parasitic elements of the package, PCB, and pad ring can introduce resonant pathways and so power and ground ringing. The drain depletion capacitance of each MOS also transmits voltage variations into the bulk. In the case of a basic inverter, the output voltage is directly coupled to the substrate through the drain depletion capacitance of the NMOS and the PMOS. Additionally, the gate electrode is coupled to the substrate through its oxide and the channel capacitance. Another noise generator is the well-known impact ionization. When a MOS transistor is biased in the saturation regime, a high electric field develops in the depleted region of the channel, near the drain. This high field creates hot carriers that dissipate their energy by generating some electron-hole pairs. For a NMOS, the holes created are swept to the substrate.

Other mechanisms exist and are described in different works: capacitive coupling with signals interconnects, gate induced drain leakage, photon-induced current and diode leakage current.

4.2.1 ICEM Standard Approach and Its Extension

In this part, we introduce a basic model to simulate the substrate voltage. We will consider the power and ground bounces as the unique source of substrate noise. This approach drastically simplifies the modeling methodology and will give, as shown hereafter, correct results. The ICEM describes the electromagnetic behavior of an integrated circuit [6,7]. Two coupling mechanisms of the internal activities for emission are proposed in this model: the conducted emissions or through input/output lines and the direct radiated emissions. The basic architecture of the ICEM model is shown in the Figure 4.2. It consists in two sub-models: a Passive Distribution Network sub-model and an Internal Activity sub-model.

The use of the ICEM allows an accurate modeling of the integrated circuit power and ground bounces [6,7]. To simulate parasitic substrate voltage induced by the supply bounces, a Substrate Network sub-model is added to the classical ICEM (Figure 4.2). The IA sub-model describes the internal
activity of the digital circuit and is represented by the transient current consumption and by the capacitance of the digital circuitry.

The PDN is the sub-model used to describe the electrical structure for powering the chip from the PCB to the on-chip power metal lines. The added module, SN, is an RC network that models the substrate noise propagation. From the existing ICEM and an additional substrate sub-model, a new methodology of electronics design optimization is shown: substrate noise characterization.

4.2.1.1 Analog Part and Substrate Coupling

The design of mixed signal ICs supposes the resolution of coupling problems between analog and digital blocks placed on the same die. The switching events of digital gates involve variations of supply voltage function in digital signal transitions that are not compensated by decoupling capacitors. Isolation between analog and digital parts with buried layers, guard rings, or separation of the supply nets are methods to reduce coupling mechanisms [7–9].
However, substrate parasitic capacitors and resistors allow the noise signal generated by the digital part to pass through the substrate and to reach the analog and radio frequency (RF) blocks. The literature is quite poor concerning the impact on analog and RF blocks, many papers being focused on noise generation and propagation into digital CMOS circuits [10–12].

This chapter deals with the impact of low frequency substrate noise onto a fully integrated VCO. We have investigated the way the substrate noise (digital noise or injected noise by means of substrate taps inside VCO core) is converted close to the carrier frequency and impacts VCO spectral purity. Simple calculations and measurements without phase noise formalism are possible as we quantify the coupling mechanism by evaluating the side-bands power relative to the carrier (in dBc). Compared to previous work [11,13], this chapter aims to locally analyze coupling mechanisms between substrate noise and the VCO spectrum as two injected points are placed inside the VCO core. We do not use a global approach by considering only power supply bounces due to coupling between substrate and power supply metal rail. We accurately analyze coupling mechanism in order to determine which devices are sensitive to bulk noise in our specific VCO test-chip, including integrated injection taps. This chapter is organized as follows. Section 4.2 presents the VCO cell structure and its layout implementation. The VCO oscillation frequency sensitivity functions of tuning voltage and bias current are measured and analyzed as the VCO static sensitivities in Section 4.3. Measured VCO spurious side-bands under injected noise perturbation are also presented. Then, simulated varactor and bipolar transistor contributions to the carrier frequency variations are analyzed in Section 4.4.

4.2.1.2 VCO Structure and Layout

The VCO was designed into a 0.35 μm BiCMOS high-ohmic process technology. Figure 4.3 shows the simplified VCO schematic. The main part of the VCO is the LC-tank. The negative resistance is obtained by a cross-coupled differential pair of hetero-junction bipolar transistors biased by an $I_{\text{bias}}$ current.

In order to inject a parasitic signal directly into the substrate with an external generator, we have placed several contacts near the differential transistors and the inductors (4). The circuit supply voltage is 3.3 V. The tuning voltage can vary from 0 V to 4 V to obtain a carrier frequency from 4.25 GHz to 4.60 GHz. The output signals pass through buffers formed by a common collector circuit configuration. The power magnitude delivered to a 50 Ω load under this current is close to 0 dBm. The phase noise measured at 100 kHz from carrier varies from –90 dBc/Hz up to –100 dBc/Hz (depending on chip dispersion and biasing). To avoid frequency variations due to supply voltage noise, many decoupling capacitors are placed in the VCO layout (Figure 4.2). For the same purpose, substrate contacts and guard rings around the devices that have a large surface in contact with the bulk have been added. Other
substrate contacts with different areas and locations are placed on the test-chip to allow us to estimate the contact and substrate resistance.

Substrate contacts for perturbation injection have different areas and locations on the chip that could allow us to estimate the contact and substrate resistance.

4.2.1.3 Static Sensitivity Functions

VCO carrier frequency variations depend on bias current and tuning voltage.

Two sensitivity functions can be used to describe the variations of the VCO carrier function of the bias current or tuning voltage. These are, respectively, $K_{\text{bias}}$ and $K_{\text{tune}}$ (see below). A change in the $I_{\text{bias}}$ current can modulate the carrier frequency in the same manner that a modification of $V_{\text{tune}}$ voltage can simultaneously change the varactor capacitance and the output frequency. In this framework, consider a sine wave perturbation superimposed on the bias current or the tuning voltage:

$$v_m(t) = A_m \cos(\omega_m t)$$ (4.1)

The carrier frequency changes according to the expression:

$$f = f_c + K \cdot v_m(t)$$ (4.2)

where $f_c$ is the VCO carrier frequency and $K$ the sensitivity function.

After frequency integration to determine the phase, the output signal of the oscillator is determined by the following equation:

$$s(t) = A \cos \left( \omega t + \frac{A_m K}{f_m} \sin(\omega_m t) \right)$$ (4.3)

The modulation index ($A_m K/f_m$) depends on a sensitivity function. For a supply voltage perturbation, the modulation index has a low value, so we can assume in our calculations that the modulation band is placed in a narrow range. We refer to the carrier in order to compute the perturbation level in the spectral domain. With these assumptions, the spectral power relative to the carrier in dBc units is given by

$$P_{\text{sbc}} = 20 \cdot \log \left[ \frac{K \cdot A_m}{2 f_m} \right]$$ (4.4)

It measures the gap between the spurious side-band power and the carrier magnitude and the parasitic side band one (Figure 4.5). A perturbation superimposed on the bias current or tuning voltage generates side-bands that have the power magnitude directly proportional to $K$ sensitivity (Equation 4.4). In the same time, $K$ sensitivity is function of the bias current and of the tuning
voltage. Thus, the noise power below the carrier varies when biasing or tuning are modified.

Figure 4.4 shows the plot of the measured VCO frequency as a function of the tuning voltage and the bias current.

In order to compare the sensitivity functions and their effects on the power below carrier when a substrate perturbation is applied, we represent the frequency evolution versus the bias current and tuning voltage on Figure 4.4. The sensitivity function is obtained by derivation of the frequency curve (see Figures 4.5 and 4.6).

Figure 4.5 represents the simulated and measured sensitivity function of the bias current. Simulations of the sensitivity functions have been made with the Cadence-SpectreRF simulator. Perturbation effect on bias current results in a small variation of the carrier frequency. The voltage applied to the varactors generates a much more important sensitivity level than the bias current sensitivity. Roughly, the sensitivity function magnitude for bias
current $K_{\text{bias}}$ is ten times lower compared to the tuning voltage sensitivity $K_{\text{tune}}$ (Figures 4.5 and 4.6).

This method lets us establish the VCO sensitivities as functions of bias circuit conditions by measurements and/or simulations. From Equation 4.4, the impact of a perturbation on bias source or tuning voltage can be easily evaluated. By these assumptions, the impact of supply noise could be reduced. VCO bias has to be properly chosen in order to decrease the VCO frequency sensitivity.
4.2.1.4 VCO Spurious Side-Bands Due to Substrate Perturbation

Experimentally, when sine wave voltage signal is injected into substrate, we measure VCO spurious side-bands closed to carrier frequency \( f_c \). The VCO sensitivity due to injected perturbation (level, location, frequency, etc.) is quantified by \( P_{sbc} \) values (Figures 4.3 and 4.7).

Substrate noise induces \( V_{ss} \) and \( V_{dd} \) power supply bounces. In our specific test-chip—considering the high-ohmic substrate (noise attenuation with distance, substrate cannot be considered as a single node), numerous on-chip decoupling capacitors, and injection nodes inside VCO—we, obviously, have a direct path between injected nodes and passive or active device bulk (varactor, inductor, HBT’s, etc.). Studying components sensitivity can be used to analyze the contribution of each one to the output noise. Simulated transfer functions between a source directly applied to the device substrate pins and VCO output have been studied (Table 4.1). The \( P_{sbc} \) simulated data shows that an important contribution to output noise is given by the devices that have a large n-well and/or n-buried layer area (varactors and transistors).

![Bias current sensitivity function (K\textsubscript{bias}).](image)

### TABLE 4.1
Component Contributions to the Output Power

<table>
<thead>
<tr>
<th>Device</th>
<th>Area\textsuperscript{a} (μm\textsuperscript{2})</th>
<th>( P_{sbc} ) (dBc)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Varactors</td>
<td>2800</td>
<td>-35.93</td>
</tr>
<tr>
<td>Inductors</td>
<td>-</td>
<td>-104.25</td>
</tr>
<tr>
<td>Transistors</td>
<td>4800</td>
<td>-5.54</td>
</tr>
<tr>
<td>Varactors and transistors</td>
<td>7600</td>
<td>-5.65</td>
</tr>
<tr>
<td>All</td>
<td>7600</td>
<td>-5.91</td>
</tr>
</tbody>
</table>

\textsuperscript{a} n-well and/or n-buried area.
A correlation between sensitive components and $P_{sbc}$ values has been established. Injection of the sine wave noise close to the bipolar transistor substrate generates important spurious side-bands. An equivalent impact is obtained when the same sine wave is injected into both bipolar transistor and varactor substrate. For similar injection conditions, bipolar substrate noise impact surpasses varactor contribution. A deep study of this correlation will be made in a future work.

To accurately simulate the impact of a substrate sine wave perturbation, some of the substrate elements based on measurements between injection contacts and grounds have been determined. The passive and active device models used for our simulations contain equations for the parasitic coupling elements. In this way, to compare measured and simulated data, it is necessary to implement elements describing coupling paths between the injection point and VCO components. The contacts used to inject noise into the substrate have different areas and are placed in different locations. The circuit devices are surrounded by substrate isolations (guard ring resistance) of different resistance values connected to the ground. Due to parasitic elements, the resistance of injection substrate contact to the ground depends on its layout location. Thus, the injected perturbation will be more attenuated when the substrate isolation (guard ring resistance) of a device has a low resistance value. With these remarks and our measurement interpretations, we created a basic substrate model by adjusting resistances from guard ring to ground and from substrate to ground for injection into the transistor, inductor and varactor substrates. Figures 4.8 and 4.9 shows the tuning voltage sensitivity and the power of the side band below carrier $P_{sbc}$ respectively as a function of the tuning voltage sensitivity. Measurements and simulations of $P_{sbc}$ have been obtained using 150 mV injection peak voltage. This sine wave has been injected near one of the inductors (Figure 4.2), at 150 kHz. These measurements show that there is a direct link between the VCO tuning voltage sensitivity and the side band power ($P_{sbc}$).

Circuit simulations in our basic substrate model show that two main devices can convert substrate noise into the output power: transistors and varactors. Converted noise by transistors versus tuning voltage sensitivity (Figure 4.10) is a roughly constant function and has an important contribution to $P_{sbc}$ level. On the other hand, converted noise by varactors leads to an important decrease of the $P_{sbc}$ with tuning voltage sensitivity. The comparison between simulated data obtained with simple substrate model and measured data proves that $P_{sbc}$ values are dominated by varactor behavior. (Increase in $P_{sbc}$ depends on tuning voltage sensitivity level). With the injection close to one of the inductors and considering the substrate attenuation, VCO side-bands are mainly introduced by the varactor sensitivity to the low frequency harmonic substrate noise. With the injection in the vicinity of transistors of the cross-coupled pair, measured $P_{sbc}$ values are higher compared to $P_{sbc}$ for injection close inductor (for the same injected perturbation) and do not depend on the tuning voltage sensitivity. This remark agrees with the simulated behavior obtained with our simple substrate model (Figure 4.8).
To confirm our approach, we use a standard BiCMOS process with 5 metal layers and a high resistive substrate. This allows us to characterize substrate noise generated by the digital part of a mixed signal integrated circuit. Figure 4.11 shows a chip microphotograph.

**FIGURE 4.8**
Tuning voltage sensitivity function ($K_{tune}$).

**FIGURE 4.9**
Measured $P_{sbc}$ function of tuning voltage (50 m Vpk at 100 kHz perturbation is injected close to inductors).

### 4.2.2 Test Chips Presentation

To confirm our approach, we use a standard BiCMOS process with 5 metal layers and a high resistive substrate. This allows us to characterize substrate noise generated by the digital part of a mixed signal integrated circuit. Figure 4.11 shows a chip microphotograph.
Four inverter networks are placed to generate noise into the substrate. They can all be driven, with many configurations, by a programmable logical command. We can switch to different numbers of inverters according to their drive or their location on the layout. This command is isolated in the substrate from the other part of the circuit by a P+ guard ring connected to a dedicated ground point. This isolation reduces the incidence of the command switching events on the measured substrate voltage. All the noisy inverters can switch in a very large frequency range, from 0 to more than 500 MHz, depending on the external clock frequency. On the same die, lies a high frequency Voltage Controlled Oscillator that should be disturbed by the digital switching noise. Many bulk taps, all over the system, allow substrate voltage measurements.
and also external noise injection; different configurations can be programmed. All these configurations make it possible to have many test cases for the comparison between measurements and simulations.

The package of the circuit is a QFN (quad-flat no-leads) with very short bonding wires and a backside or slug contact. This kind of package is currently used for low-noise or RF applications.

4.2.3 Extractions, Simulations, and Experimental Results

4.2.3.1 ICEM Model Parameters Extraction

The extended-ICEM model of our test-chip is composed of five main parts: the PCB supply lines, the socket and the package, the supply lines of the chip, the core of each digital part of the circuit, and the simplified substrate model. The parasitic inductances, capacitances and resistances of supply lines are extracted from layouts and 3D models with different dedicated tools [14–17]. Those tools provide us an equivalent RLC network of each part. Figure 4.12 gives an equivalent RLC lumped network that can be used to model two adjacent bonding wires. This schematic is a good example of how the different parts of the supply lines can be modeled. Typical values of such model parasitic elements are: \( L_{\text{bond1}} = L_{\text{bond2}} = 1.45 \, \text{nH} \), \( C_{\text{bond1}} = C_{\text{bond2}} = 5.1 \, \text{fF} \), \( C_{\text{bond12}} = 67 \, \text{fF} \) and \( K_{12} = 0.26 \).

The core consumption current is a waveform obtained with SPICE transient simulations of each block. The core capacitance is also provided from AC Spice simulations. This capacitance can also be approximated by adding the capacitances of all the logical gates included in the digital design. Lastly, the substrate model is extracted from a simplified layout with a CAD tool substrate extractor [14–17]. We obtain, after a long step of extraction, a SPICE netlist of the substrate that can be linked in the global simulation schematic. The measurement lines have also been modeled in order to consider the different parasitic elements that should be disturbing for measurements.

![FIGURE 4.12](image)

Adjacent bonding wires RLC model.
4.2.3.2 Measurements and Simulations

The comparisons confirm the effectiveness of the proposed simulation method. Different configurations are tried by changing some important parameters in substrate noise generation or propagation: the power magnitude of injected noise, the transfer function of the package, and the location of the measurement substrate contact.

When high current spikes are requested by the inverter networks, the simulation results are more pessimistic than the measurements. This is mainly due to the consumed current characterization step. During this step, power supply and ground lines are supposed to be perfect; thus, the voltage drop effects are not simulated.

Another way to validate this simple model is to change the transfer function of the package by cutting off some power bond wires. The chip has three dedicated power bond wires in the classical configuration. To show the effectiveness of the extended-ICEM model, we have kept only one power bonding wire. Figures 4.13 and 4.14 still show good correlations.

Levels measured are quite similar between both bonding configurations. As expected, frequencies decrease when only one power supply bond wire is

![Figure 4.13](image1.png)

**FIGURE 4.13**
Comparisons between measurements and simulations of the substrate voltage generated by the networks of reversers “1” and “2” on the extnoise4 measurement plot to show defects of the simulated model.

![Figure 4.14](image2.png)

**FIGURE 4.14**
Comparisons between measurements and simulations of the substrate voltage generated by the networks of reversers “3” and “4” on the extnoise4 measurement plot to show defects of the simulated model.
kept. This is due to the increase of the power supply line parasitic inductance that involves the down-shifting of the resonance frequency.

Finally, we can also measure the substrate voltage on different P+ contacts at different points of the die. The resistance between the ground and the substrate tap depends on its location. The first contact is closer to the system ground than the second one; as a consequence, the peak to peak substrate voltage measured on the first contact is higher than the second substrate contact measurement. These simulations follow measurements and still confirm the effectiveness of the test-chip simulation schematic.

4.3 Overview of the 3D Interconnect and Substrate Modeling Approach

4.3.1 The Different Steps of the Modeling Approach

3D interconnects require the consideration of the global electrical context to correctly evaluate system performances. We propose physics-based compact models derived from semiconductor and electromagnetic theory. At first, the models are derived from parametrical extractions performed on test structures. The $RLCG$ parametrical extractions are performed on wafer through $S$-parameters measurements with a Vector Network Analyzer (VNA) and ground-signal-ground probes (SOLT calibration) for a frequency sweep from 70 kHz to 40 GHz. The Thru-Reflect-Line (TRL) de-embedding technique is applied to remove the contact and access lines effects from the $S$-parameters measurements and, thus, obtain the test structures actual RF behaviors \[12\]. A more physical modeling approach relies on analyzing the test structures afterwards by means of: (1) a 3D full-wave electromagnetic tool using the Finite Element Method (FEM) to understand the physical and electrical phenomena occurring in 3D interconnects during the propagation of a signal, and (2) the Transmission Line Method (TLM).

TSVs cannot always be considered as perfect cylinders. Diameter increases toward the TSV top surface (BEOL [back end of line] level) while the thicknesses of the copper and oxide layers decrease. For a W1 configuration (e.g., Figure 4.15), the TSV diameter, including the copper layer and the polymer material, varies from 60 μm to 59 μm. In a W2 configuration, the diameter varies from 40 μm to 37 μm. At each extremity, for both configurations, the TSV copper and SiO$_2$ layers thicknesses vary respectively from 1 μm to 3 μm and from 0.2 μm to 0.5 μm (W1 and W2 configurations).
4.3.1.1 Compact Models of the Medium-TSV (and Coplanar Line)

As in planar technologies, 3D interconnects can be built with \(RLCG\) passive components described in \(\Pi\) or T networks. It does not matter which type of network is chosen as long as the interconnect length is much smaller than the length of the propagated signal wavelength.

Otherwise, both have to be distributed in a certain number of \(RLCG\) elementary cells to give an equivalent response. We consider the T network in the rest of this chapter. Each of the 3D interconnect \(RLCG\) networks is modeled with serial elements (resistances or partial inductances) to model the signal propagation, and parallel elements (capacitance or conductance) and to model the interconnect environment. The proximity (or coupling) effects are also included in the compact model description. The coplanar line resistances and the self- and mutual- inductances are calculated from some well-known formula [14].

The resistances are calculated for a DC value (the skin effect could be considered later) and the inductances are calculated depending on the partial inductance analytical expressions [18–21].

The compact models that we propose works in low and medium frequencies for medium density TSV. We have chosen to calculate resistances with DC values.

\[
R = \rho \frac{L}{W \cdot T} \tag{4.5}
\]

\[
L_{\text{self}} = \mu_c \frac{L}{2\pi} \left[ \ln \left( \frac{2L}{W + T} \right) + 0.5 + \frac{0.447(W + T)}{2L} \right] \tag{4.6}
\]

\[
M = \mu_c \frac{L}{2\pi} \left[ \ln \left( \frac{2L}{p} \right) - 1 + \frac{p}{L} \right] \tag{4.7}
\]
where $\rho$ is the metal resistivity (copper: $1.72 \times 10^{-8}\,\Omega\cdot m$); $\mu$, the copper permeability; $W$, $L$, $T$ and $P$, respectively, the line width, length, thickness and the pitch between two interconnect lines (Figure 4.7).

The interline capacitance $C_{\text{inter}}$ (or coupling capacitance) is calculated according the set of equations defined as function of the concerned line surfaces and the fringe capacitances taken at the extremities ($C_f$) and the middle ($C_f'$) of the coupled-line system. The electrical parameter $C_p$ corresponds to the coupling capacitance between the ground plane and the concerned line surface (Figure 4.16). It is referred in the literature as the line’s self-capacitance.

\[
C_f = \varepsilon_{\text{ox}} \left( 0.075 \frac{W}{H} + 1.4 \left( \frac{T}{H} \right)^{0.222} \right) \quad (4.8)
\]

\[
C_f' = \frac{C_f}{1 + (H/S)} \quad (4.9)
\]

\[
C_p = \varepsilon_0 \varepsilon_{\text{ox}} \frac{W \cdot L}{H} \quad (4.10)
\]

\[
C_{\text{inter}} = C_f - C_f' + \frac{\varepsilon_{\text{ox}} L}{100} \left( 3 \frac{W}{H} + 83 \frac{T}{H} - 7 \left( \frac{T}{H} \right)^{0.222} \right) \cdot \left( \frac{H}{S} \right)^{1.24} \quad (4.11)
\]

where $\varepsilon_{\text{ox}}$ is the silicon oxide permittivity and $S$ is the inter-line gap. An average value of the $W$ width in the formula is used, the signal and ground lines having different widths.

We propose our own analytical expressions for the calculation of the medium-density TSV compact model resistance and oxide capacitance. The

\[FIGURE 4.16\]
Illustration of the capacitive couplings between parallel lines located over a ground plane.
TSV being conical, the expressions are derived from the formula defining a perfect cylindrical conductor, for which we have applied, along the conductor length, linear variations for the thickness and radius.

\[
R_{TSV} = \frac{H}{\pi \sigma} \frac{1}{2(R_{mt} \cdot T_{md} - R_{md} \cdot T_{mt})} \ln \left( \frac{T_{md}}{2R_{md} - T_{mt}} \right) \tag{4.12}
\]

\[
C_{ox(TSV)} = \frac{\varepsilon_0 \varepsilon_{ox} \cdot 2\pi \cdot H}{T_{ot} - T_{od}} \left[ R_{ot} - R_{od} + \frac{R_{ot} \cdot T_{od} - R_{od} \cdot T_{ot}}{T_{ot} - T_{od}} \ln \left( \frac{T_{od}}{T_{ot}} \right) \right], \tag{4.13}
\]

\[
R_{ot} = R_{mt} + T_{ot}, \quad R_{od} = R_{md} + T_{od}
\]

where \( R_{mt} \) and \( T_{mt} \) are the copper layer radius and thickness of the TSV top surface, \( R_{ot} \) and \( T_{ot} \) are the oxide layer radius and thickness of the TSV top surface, \( R_{md} \) and \( T_{md} \) are the copper layer radius and thickness of the TSV bottom surface, and \( R_{od} \) and \( T_{od} \) are the oxide layer radius and thickness of the TSV bottom surface.

According to the geometrical data, supposing the W1 configuration: \( R_{mt} = 30 \mu m, R_{md} = 29.5 \mu m, T_{mt} = 1 \mu m, T_{md} = 3 \mu m, T_{ot} = 0.2 \mu m, T_{od} = 0.5 \mu m. \)

The polymer material filling the TSV does not significantly affect its RF behaviour. Besides, the variations of the TSV radius and the copper layer thickness are very low. Consequently, the analytical expressions of a filled cylindrical conductor are still used in order to calculate the self and mutual inductances.

\[
L_{TSV} = \mu_0 \mu_r \frac{H}{2\pi} \left[ \sinh^{-1} \left( \frac{H}{R_a} \right) + \frac{R_a}{H} + 0.15 + \sqrt{\left( \frac{R_a}{H} \right)^2 + 1} \right] \tag{4.14}
\]

\[
M_{TSV} = \mu_0 \mu_r \frac{H}{2\pi} \left[ \sinh^{-1} \left( \frac{H}{p} \right) + \frac{p}{H} - \sqrt{\left( \frac{p}{H} \right)^2 + 1} \right] \tag{4.15}
\]

where \( p \) is the pitch between two nearby TSVs and \( R_a \) the TSV average radius.

### 4.3.1.2 Global Electrical Context Modeling

The modeling of the global electrical context is illustrated for TSV chains and for CPWs (coplanar wave guides), the latter of which will not be presented here. In the TSV chain, the currents propagate vertically through the epitaxial and the oxide layers to reach the ground planes corresponding to the BEOL level ground lines (Figure 4.15). The epitaxial and oxide layers electrical parameters \( (R_{epi(TSV)}, C_{epi(TSV)}, \text{ and } C_{ox(GND)}) \) are calculated in
the same way as the coplanar waveguide. The couplings between the substrate and the TSVs are taken into account with the geometrical capacitance $C_{ox(TSV)}$. Only the proximity effects between TSVs (TSV/TSV couplings) are considered. The TSV chain electrical context modeling involves dividing the BEOL ground lines into serial blocks, by dissociating, on the overall surface, the parts reached by the current coming from the TSVs.

These surface parts have a length corresponding to the TSVs contact pads length $L_{pad}$. The epitaxial layer parameters ($R_{epi(TSV)}$ $C_{epi(TSV)}$) and the oxide capacitance ($C_{ox(GND)}$) which model the current propagation to the ground line through the TSV, must therefore be calculated for $L = L_{pad}$.

The ground lines surfaces parts involved in the current paths are simply modeled by $RL$ networks.

### 4.3.1.3 To a Simulation Platform

#### 4.3.1.3.1 Substrate Modeling Approach

The main difficulty with a priori exploration is that the choice of architectural block parameters must be made according to non-ideal effects (implementation technology, sensitivity to noise and temperature variations, dispersion), which are not known here. It is therefore essential to determine the application-defined design space and to map this to a technology-defined (see, e.g., Figure 14.8) design space for each architectural variant to be considered. The development of this approach will thus rely heavily on high-level models, as well as on design database exploitation (data mining techniques and the suitability of Pareto fronts has to be investigated to optimize the search speed and database size) and estimation methods. This in

![FIGURE 4.17](image)

Left: Medium-density TSV front view. Right: RLCG compact modeling of the medium-density TSV including the current path.
combination with bottom-up performance space models as a way to improve the overall efficiency of the flow will be investigated.

Commercially available EDA (Electronic Design Automation) tools are required to allow a flexible floor plan and better vertical and horizontal place and route steps, including better thermal modeling and specific DFY (Design for Yield) constraints. Design rules have to be derived and provided to the designer using simulation results and, when possible, measurement data. These rules are related to optimize the thermal management of the structure and minimize crosstalk, signal delays, electro-thermal interactions, losses at the RF domain, etc. Parametric simulation studies will also be carried out to derive the rules. Among others, parameters are geometry, materials used, and material properties.

Currently, EDA tools supporting IC package, module and SiP design are architected in a way that supports and assumes all connections between dies going through IC package fabrics (e.g., bumps, wire bonds, traces and vias, or package-on-package [PoP] solder balls).

With emerging request for 3D die stacking, this assumption is no longer valid. In order to support 3D architectures, EDA tools will have to be improved to handle direct die-to-die connections within the IC layout tool, including the support of stacked chip configuration, connectivity management, parasitic extraction, analysis, and simulation of the stacked IC.

Methodology, flow, and tools ought to be developed to allow flexible stacked IC connectivity between different ICs and also the final package. Different styles of connectivity will be defined and supported to allow greater cost-efficiency and better electrical and thermal results.

The definition and implementation of new methods for flexible floor plan generation, vertical placing and complex models for interconnects, power grid and clock routing are needed.

**FIGURE 4.18**
Left: Specific depth profile (p+/p-region). Right: 3D schematic of the structure.
So we will develop an EDA flow for the following:

1. Define TSV and contacts placement and automatic alignment and update driven from top/bottom die.
2. Define the power network based on TSV and contact direct connection to the power grid.
3. Provide timing analysis of the interconnections through various configurations, such as TSV, stacked dies, and face to face interconnection. This will be based on standard RC parasitic extractions and static timing analysis.
4. Generate a thermal model of a system composed of several dies to be used later in package and PCB simulation.
5. Generate an electrical model of a system composed of several dies to be used later in package and PCB simulation.

4.3.1.3.2 General Design Flow

TSV-based stacked IC design methodology requires a comprehensive development of both the existing flow approach and a totally new development of the design flow and its associated tools.

The TSV design flow development shall initially be developed according to the baseline approach (Figure 4.19).

![Design Flow synopsis](image)

**FIGURE 4.19**
Design Flow synopsis.
4.3.1.3.3 Transmission Line Extractor 3D-TLE

When we consider the global electrical context (e.g., substrate impedance) and the compact model’s distribution, the total compact model can become very complex. So, we develop a 3D extraction tool, 3D-TLE (3D Transmission Line Extractor), based on our proposed approach, which integrates the substrate extraction method algorithms.

The modeling of a conductive substrate as a simple node is only viable for low and medium frequency domains. At high frequency, the substrate coupling effects must be added to the system electrical modeling by representing the substrate as a RLCG network to more accurately evaluate the IC’s losses. The modeling can become rapidly complex since the coupling effects must be considered between all the components of the chip. Moreover, the substrate can be non-uniform with different doping values, that is, having different resistivity and permittivity throughout the considered volume. The substrate is therefore modeled as a stack of parallel heterogeneous dielectric layers, because the doping profile evolves in the perpendicular direction to the Si–SiO₂ surface. The extraction tool generates, from this text file, a SPICE net list containing the system RLCG electrical description, which can be exported to EDA tools such as Agilent Technologies ADS®. The viability of 3D-TLE was checked through comparisons with COMSOL (FEM) simulations.

4.3.1.3.4 Input Txt File Geometrical Description

The file is composed of four classes: the layers, components, paths, and couplings. The layers represent the basic information about the layers, the components define every single component, the paths represent the interconnections, and the couplings define the coupling relationship.
4.3.1.3.5 Layers

We can see substrate layers definition in Table 4.3. In this table, the type of layers can be SUB (substrate), OXI (oxide), EPI (epitaxial), RDL (redistribution layer), and BEOL (back-end-of line). But for RDL and BEOL, they have a different definition, as shown in Table 4.4.
4.3.1.3.6 Devices

We can see devices description in Table 4.5.

<table>
<thead>
<tr>
<th>TABLE 4.5</th>
<th>Devices Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Type of components</strong></td>
<td><strong>Number of components of the same type</strong></td>
</tr>
<tr>
<td>LINE</td>
<td>1</td>
</tr>
<tr>
<td>TSV</td>
<td>1</td>
</tr>
</tbody>
</table>

Here the type of components can be LINE, TSV, and TSVPORT. But for TSV, the description is a little heavier.

4.3.1.3.7 Paths

For paths, we can see a definition in Table 4.6.

<table>
<thead>
<tr>
<th>TABLE 4.6</th>
<th>Interdevices Path Description [7]</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Type of components</strong></td>
<td><strong>Number of paths of the same type</strong></td>
</tr>
<tr>
<td>LINE</td>
<td>1</td>
</tr>
<tr>
<td>TSV</td>
<td>1</td>
</tr>
</tbody>
</table>

Here, the type of components can be LINE, TSV, and TSVPORT, which are predefined in the former part. Type of paths can be signal, GND, RDL, and pad for TSVPORT, TSV for TSV. If the component is coupled with other...
components in the path's description, it will be added as "coupled" at the end. The coupling relationship will be defined in the following part "coupling."

4.3.1.3.8 Coupling

TABLE 4.7

<table>
<thead>
<tr>
<th>LINE</th>
<th>gnd1</th>
<th>LINE</th>
<th>gnd2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type of component</td>
<td>The exact coupling component</td>
<td>Type of component</td>
<td>The exact coupling component</td>
</tr>
</tbody>
</table>

3D-TLE will automatically generate a 3D structure in the geometry block, a schematic in the schematic block, and a SPICE-compatible txt file. Its content will be displayed in the result block (Figure 4.21).

4.3.1.3.9 Substrate Extractor

The layered substrate is often treated as a simple node, but, at high frequency, the substrate coupling effects must be added to the system electrical modeling.

Our extractor is developed to analytically extract the RC network and to more accurately evaluate the IC’ losses. With an affordable speed, the substrate extractor can be divided into five parts. The upper-left corner block defines the general study information, which includes the study frequency domain, the number of study frequency points per decade, the dimension

FIGURE 4.21

3D TLE simulation platform.
of the substrate, the mesh scale with 1 μm as reference, and the study mode— that is, contact–contact mode, TSV–contact mode, and TSV–TSV mode (contact–contact mode studies the cases where the contacts are embedded in the substrate. TSV–contact mode extracts the RC parameters between an insertion TSV and a contact embedded in the substrate and TSV–TSV mode performs the RC extraction of 2 TSVs inserted in the substrate [22]. The upper-middle block defines the TSV or contacts geometries. The lower-left block defines the layers’ physical characteristics, like the conductivity, thickness, and relative permittivity [23]. Once we define the geometries, we can click on the draw figure button in the middle of the interface and it will automatically generate the 2D section image. The extracted RCZ result will be shown in the right section. Here is a TSV–contact extraction result.

4.4 Conclusion

We propose a compact and pragmatic modeling approach to the entanglement of 3D substrate and its interconnects. For interconnects, the modeling approach is applied to redistribution lines and medium-density TSVs. It is based on parametrical extractions performed on realistic test structures and analytical formulas. Moreover, it includes the system global electrical context with the current paths and the modeling of proximity and/or substrate effects. Complete equivalent electrical models are illustrated for TSV chains structures. The modeling approach gives finally some equivalent electrical models. However, while it implies the modeling of all the substrate coupled effects existing between the elements sharing this substrate, it still requires an external substrate substrate coupling simulation method.

This chapter proposes a substrate coupling simulation method suitable for execution in a conventional CAD environment. A standard approach called ICEM (Integrated Circuit Emissions Model) has been extended to allow fast substrate noise simulations. Currently, this model considers only the noise generated in the substrate by the power supply and ground bounces. A more complex model is needed to integrate other injection phenomena, such as impact ionization or drain coupling, for instance. Moreover, to apply this approach to a realistic mixed signal design several challenges have to be grasped. The first one concerns the way to obtain the transient consumption current of an entire large digital part. Some CAD tools offer the possibility to simulate these currents. Finally, it is necessary to analyze influenced analog device of interest, such as VCOs disturbed by parasites coming often from digital block via the substrate.

The impact of low frequency substrate noise on a typical RF analog device, a voltage-controlled oscillator, is studied. At first, we presented the test-chip structure with fully integrated VCO and two substrate taps inside the VCO core for noise injection or measurement (one close inductor/varactor and the other in vicinity of the HBT cross-coupled pair). VCO characterization is performed through measured static sensitivity curves that represent the
frequency variations function of tuning voltage or bias current. An analytical approach to harmonic perturbation superimposed on bias current or tuning resumes the classical frequency modulation mechanism with observed spurious side-bands. Then measured VCO side-bands are analyzed when harmonic voltage noise is injected.

The next step was the study of the sensitive devices. Many simulations were carried out with a simple substrate model, leading to the conclusion that mainly varactors and bipolar transistors are affected by substrate noise. These simulations agree with the measurements: side-band power below carrier is more important when the injection is located close to the HBT’s of the cross-coupled pair and does not depend on the tuning voltage. On the other hand, side-band power below carrier decreases with tuning voltage when the injection is located close inductor and varactor. Finally, we demonstrate that there is a direct link between the VCO tuning voltage sensitivity and the side-band power. Output noise power is a function of circuit sensitivities and device isolations. Furthermore, we explicitly show, in this chapter that a global approach, since it only considers resistive and/or capacitive coupling between substrate and power supply rails, is not sufficient for precise quantification of noise impact on the radio frequency oscillator.

Moreover, the ICEM model has been tested for contact pads, coplanar waveguides and TSV structures. This simple approach has the advantage of being easily automated. Additionally, the model can be improved by including skin effect and eddy current. On-going works will consist of extending the modeling approach to other types of 3D interconnects, such as copper pillars, and to different types of 3D interconnect matrices.

Last of all, we begin to build a simulation platform dedicated to substrates with their connectics. The user describes his system in a text file by means of specific hierarchical syntax and statements. He declares the system as a subcircuit with a certain number of input/output ports (there is no limitation in number). The subcircuit contains components connected with internal nodes. Instead of defining RLCG components with resistance/inductance/capacitance/conductance values, the user defined structures such as lines, pillars, TSVs, or CPWs with associated parameters corresponding to the technological and/or geometrical data. He can specify whether the structures in the subcircuit are coupled or not, possible current paths, and so on.

Once the user has finished its system/subcircuit description, he loads it in our 3D-TLE simulator and launches the extraction tool. Then, 3D-TLE provides, as an output file, a SPICE-like format netlist of the subcircuit, in which all the components are described electrically with RLCG parameters. These electrical RLCG structures correspond to the compact model that we proposed. The I/O ports of the subcircuit are the ones declared by the user in his text file. If necessary, in addition to the internal node indicated by the user in his subcircuit description, 3D-TLE generates automatically extra internal nodes to connect the structures to the I/O ports in the SPICE netlist.

The netlist is exportable to CAD tools like ADS [24] or Cadence Virtuoso [25]. In the case of ADS, by means of different options, the user can create
from the SPICE netlist a black box containing the netlist and for which the I/O ports are the subcircuit ones.

When descending into the black box, the user is able to visualize the SPICE description and can also modify it. After generating the black box, the user instantiates it in his top level schematic. The viability of 3D-TLE is checked by comparing, for a given system, the simulated S-parameters of its 3D-TLE SPICE netlist with the ones of its electrical schematic designed under ADS®. Obviously, the expected results show some good fits describing the system, since using 3D-TLE seems easier and faster than designing it using a standard CAD tool.

Acknowledgments

This work is supported by INFIERI (Intelligent Fast Interconnected and Efficient Devices For Frontier Exploitation In Research And Industry) European Program and by UPM (Union Pour la MEDITERRANEE), and One of Us (Yue Ma). Thanks to the China Scholarship Council (CSC).

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