5 Improvement and Applications of Large-Area Flexible Electronics with Organic Transistors

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CONTENTS

5.1 INTRODUCTION

With the advantage of the circuit integration on a plastic thin film with a low-temperature, low-cost, printable or printing process, organic transistor is widely recognized as a promising candidate for realizing large-area flexible electronics such as displays [1–3], power/data transmission sheets [4,5], and sensor arrays [6–8]. The technology of organic transistors has been significantly improving.

First of all, the improvement of process maturity and yield realizes highly integrated circuits such as an 8-bit microprocessor and analog-to-digital converters (ADCs) [9–11]. For the low-voltage operation, a self-assembled monolayer (SAM) technology lowered the operation voltage toward 1 V [12]. The fastest n-type metal–oxide–semiconductor (nMOS) transistors with C_{10}-DNTT [13] achieved the signal propagation delay of 420 ns per stage in the ring oscillator at supply voltage of 3 V [14]. For high-frequency applications, some radio-frequency identifications (RFIDs) have been proposed [15,16]. Those are implemented with only high-voltage p-type metal–oxide–semiconductor (pMOS) transistors because the mobility of nMOS transistors is much slower than that of pMOS. To address this issue, a hybrid organic (pMOS)/solution-processed metal–oxide (nMOS) RFID tag was recently proposed [17]. However, the operating speed of organic transistors is still not sufficient for the operation at hundreds megahertz order even if high voltages of 20 V or higher are supplied to the circuit. Therefore, the system-level integration of organic transistors and silicon complementary metal–oxide–semiconductor (CMOS) circuits is one of the practical solutions [18].

This chapter briefly surveys recent progress of organic transistor technologies. In addition, examples of large-area flexible electronic applications, such as an electromagnetic interference (EMI) measurement sheet [18], a user customizable logic paper (UCLP) [19], a pedometer with energy harvesters [20], and 100 V AC Energy Meter [21] are introduced.

5.2 RECENT PROGRESS OF ORGANIC TRANSISTORS

Organic pMOS transistors have been getting better yield and time-dependent reliability, and therefore highly integrated organic pMOS circuits were presented such as an 8-bit microprocessor and ADCs. In terms of low-voltage operation, SAM realized 1–3 V operation enabling direct silicon-organic circuit interface in [18]. In terms of printed electronics, some printed CMOS circuits were presented [21–24]. This section introduces resent progress of technologies of organic transistors and their circuit blocks briefly.

5.2.1 8-Bit Microprocessor on Plastic Foil

The improvement of yield of organic pMOS transistors enables the integration of thousands of transistors, and an 8-bit microprocessor on a plastic foil for the first time is presented [9]. As there are no previous organic processors, the comparison with Intel 4004 processor is provided in the last resort [9]. It is, however, interesting that the first organic processor is with shorter gate length and lower operation voltage than those of Intel 4004 processor. The core of processor, an 8-bit arithmetic and logical unit (ALU), consists of NAND gates and inverters in 5 μm organic pMOS process. The processor operates with 40 Hz clock at V_{DD} of 10 V. Number of transistors (area) of the processor foil and the running averager instruction code foil are 3381 (1.96×1.72 cm^2) and 612 (0.72×0.64 cm^2), respectively. Although the performance should be improved for practical applications, it shows good technical feasibility of the organic microprocessor.

5.2.2 Fully Integrated ΔΣ Analog-to-Digital Converter

A continuous time ΔΣ ADC with 5 μm organic pMOS transistors was presented [10]. It is a fully integrated organic ADC for the first time. The V_{TH} mismatch of input differential pair transistor in an operational amplifier is a critical issue for an analog circuit, because its offset voltage directly degrades the performance. In silicon circuits, the common centroid layout will improve the matching properties. On the contrary, it is not sufficient for organic circuits. To compensate V_{TH} mismatch of input differential pair transistors in the amplifier, the circuitry employs back-gate biasing. By using the mismatch compensation scheme, the gain of the operational amplifier (opamp) is also improved. Measured SNR and bandwidth of ADC are 26.5 dB and 15.6 Hz, respectively. Clock frequency is 500 Hz at V_{DD} of 15 V. The circuit consists of 129 transistors in 13 × 20 mm^2 area. Now the performance of the ADC is mainly limited by the opamp gain of 23 dB. On the other hand, a 40 dB gain organic amplifier was recently reported by another research group [22]. This fact is attracting attention for further improvement of the organic ΔΣ ADC.

5.2.3 Low-Voltage Organic Complementary Metal–Oxide–Semiconductor Circuit

A low-voltage organic CMOS circuit using SAM-dielectric gate oxide was presented [12]. The gate oxide consists of two layers, a 1.8- to 3.8-nm-thick aluminum oxide layer and 2.1-nm-thick SAM. The nanometer-order gate oxide thickness realizes 1.5–3 V operation, which is around 10 times lower than that of conventional organic transistors. Semiconductor materials for pMOS transistors and nMOS transistors are pentacene and hexadecafluorocopperphthalocyanine (F16CuPc), respectively. This improvement enables a direct silicon-organic circuit interface in [18]. The fastest low-voltage nMOS transistors with SAM and C_{10}-DNTT [13] achieved the signal propagation delay of 420 ns per stage in the ring oscillator at supply voltage of 3 V [14].

5.2.4 Fully Printed Organic Circuit

There are several approaches to realize fully printed organic circuits. A pMOS ring oscillator is proposed that aims fully printed circuits not only devices but also interconnection [23]. On the other hand, a complete printed organic CMOS technology on a plastic foil was proposed [24]. The devices are fabricated by 5 μm line/space resolution screen-printing process and annealing at 100°C. Oscillation frequency of a seven-stage ring oscillator that consists of W/L = 1000/20 μm CMOS transistors varies from 70 Hz at 40 V to 16 Hz at 20 V. A 4-bit ADC implemented with fully printed organic CMOS [25] was presented [11]. Although they use a sputter and laser ablation processes for the 30-nm-thick gold metal layer forming, CMOS transistors themselves are printed, and therefore the first printed ADC on a flexible substrate is claimed. The ADC consists of more than 100 CMOS transistors and an

integrated resistive DAC in 24.5 cm^2 area. Measured bandwidth and SNDR are 2 Hz and 19.6 dB SNDR, respectively.

5.3 LARGE-AREA FLEXIBLE ELECTRONICS APPLICATIONS

This section introduces some examples of large-area flexible organic electronics such as an EMI measurement sheet, a UCLP, an insole pedometer with piezoelectric energy harvester, and a 100 V AC energy meter.

The EMI measurement sheet demonstrates a direct silicon-organic circuit interface for the first time. A 0.18 μm CMOS silicon large-scale integration (LSI) chip directly drives a 2 V organic CMOS circuitry through a stretchable interconnection. USLP consists of the 2 V organic CMOS circuits and ink-jet printed interconnections on a piece of paper and provides a new field customizability to users. The insole pedometer also employs the 2 V organic transistors driven by small DC power generated by piezoelectric films. These three applications have a similarity of utilizing the advantages of 2 V organic transistors. In contrast, the 100 V AC energy meter employs 20–100 V organic transistor. The drawback that the device requires high-voltage power supply is now turned to its advantage because the energy meter should handle high voltages. In this section, details on the above-mentioned applications are described.

5.3.1 A Stretchable Electromagnetic Interference Measurement Sheet

EMI that degrades the dependability of electronic devices is becoming a serious issue. As modern electronic devices have 3D structures and the packaging is dense, it is difficult to analyze the EMI generation points in electronic devices such as mobile phones and large flat-panel displays. EMI largely depends on the circuit board layout. Localizing either an EMI source or a critical wiring is difficult by simulation. EMI measurement is, therefore, important for the development of electronic systems. However, there is no method of measuring EMI on the surface of 3D structures. In the conventional method, a pencil-like magnetic-field probe with X–Y scanning equipment and spectrum analyzers are used for the EMI measurement [26]. In the method, the surface of the electronic device should be scanned repeatedly with the probe. However, the scanning equipment can only move in a flat plane. In another conventional method, a measurement system with an integrated array of magnetic-field loop antennas is used [27]. Although the method captures the distribution of a magnetic field, it is not applicable to 3D structures as the antenna array is implemented on a flat and rigid printed circuit board (PCB). To solve this problem, an EMI measurement sheet [18] was proposed, which enables the measurement of EMI distribution on the surface of 3D structures by wrapping the devices with the measurement sheet. Once EMI noise is roughly localized with the measurement sheet, one can easily scan EMI noise using the probe method for precise localization or better quantification of the electromagnetic field. The sheet can measure not only a magnetic field but also an electric field suitably by simply changing its antenna connection [18].

Figure 5.1 shows a prototype of the stretchable EMI measurement sheet. Each PCB includes 2 × 2 antenna coils and a silicon EMI measurement LSI. The sheet consists of 4 × 4 PCBs, and therefore 8 × 8 antennas are located in 12 × 12 cm^2 area. The antennas and LSIs are controlled using 2 V organic CMOS decoder and selector.

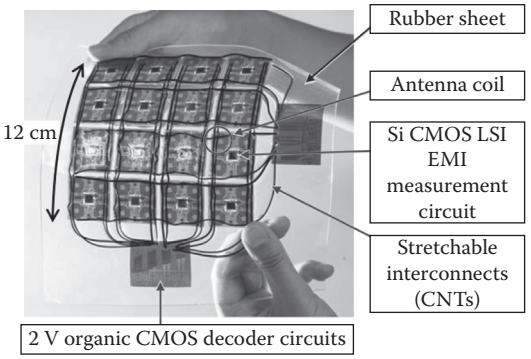


FIGURE 5.1 Stretchable electromagnetic interference measurement sheet. (K. Ishida et al., Stretchable EMI measurement sheet with 8 × 8 coil array, 2 V organic CMOS decoder, and 0.18 μm silicon CMOS LSIs for electric and magnetic field detection, *IEEE Journal of Solid-State Circuits*, 45(1), 249–259, © 2010 IEEE.)

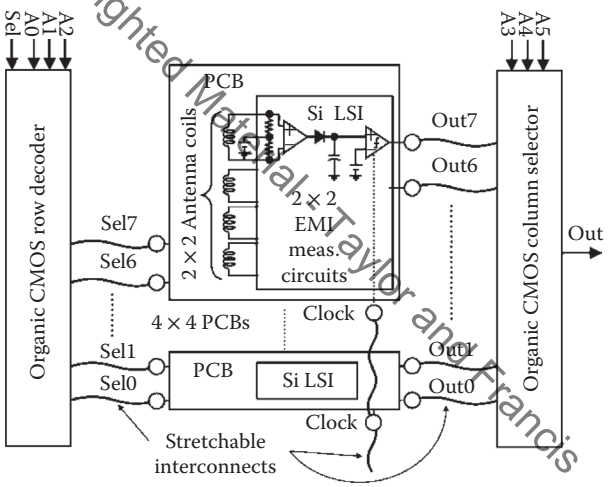


FIGURE 5.2 Block diagram of the electromagnetic interference measurement sheet. (K. Ishida et al., Stretchable EMI measurement sheet with 8 × 8 coil array, 2 V organic CMOS decoder, and 0.18 μm silicon CMOS LSIs for electric and magnetic field detection, *IEEE Journal of Solid-State Circuits*, 45(1), 249–259, © 2010 IEEE.)

Each module is electrically connected with a stretchable interconnect made of carbon nanotubes (CNTs) [28]. The overall system is sealed with a rubber sheet made of silicone elastomer. The sheet is, therefore, flexible and stretchable. Figure 5.2 shows the block diagram of the EMI measurement sheet. Three-bit address and select signals are applied to the organic CMOS row decoder. The decoder selects one row of the arrayed EMI measurement circuit. Each select signal is connected to a PCB with rubber-like stretchable interconnects. Each PCB has a 2 × 2 antenna array to pick up EMI, an LSI, and six stretchable interconnects. The four antennas share the LSI to measure EMI. The outputs of silicon LSIs are connected to the organic CMOS column selector with

stretchable interconnects. In the conventional integrated array of magnetic-field antennas on a solid board, the processing function of the measured results is not integrated in the board. In contrast, the EMI measurement sheet has the LSIs distributed near the antennas for EMI measurement. It is the first demonstration of a distributed in situ EMI measurement, which has a potential to improve the measurement speed and accuracy. The diameter of the loop antenna is 9.8 mm. The antennas are made on a rigid PCB, because the antennas on a flexible film provide unstable antenna characteristics depending on the mechanical bending. When the scale of the array is large, a low-cost and large-area decoder is required to reduce the number of interconnects, and therefore organic transistors are suitable for the decoder. The performance of the sheet will improve as the operational speed of organic devices improves. In particular, a faster row decoder and column selector will realize high-speed scanning of the array.

The system-level integration of silicon CMOS technology, 2 V organic CMOS technology [12], and stretchable interconnects including CNTs makes a stretchable EMI measurement sheet possible, and the proposed LSI demonstrates EMI noise measurement up to 1 GHz using a rectifier and comparator operating at only 100 kHz. By changing the connection of the antenna to the LSI, the electric and magnetic fields are successfully measured separately. The minimum detectable magnetic-field noise power is −70 dBm and the maximum detectable noise frequency is 1 GHz. The minimum detectable electric-field noise power is −60 dBm and the maximum detectable noise frequency is 700 MHz.

5.3.2 User Customizable Logic Paper

UCLP is proposed for both prototyping of larger-area electronics and educational applications [19]. In particular, learners can study and experience the operation of integrated circuits by fabricating custom integrated circuits, using at-home ink-jet printers to print conducting interconnects on paper that contains prefabricated arrays of organic transistors. The feasibility of UCLP is demonstrated with the newly proposed sea-of transmission-gates (SOTG) of organic CMOS transistors, providing field customizability through the use of the printable electronics technology. UCLP is applicable to a wide range of products of printable electronics including flexible displays and electronic paper, as well as for educational purposes. This technology provides a new means to add programmability for integrated circuits used in large-area electronics. Figure 5.3 shows a prototype of UCLP [19]. In UCLP, paper that contains an array of vias and an organic SOTG film are stacked.

Figure 5.4 shows the cross-sectional view of UCLP. The 2 V organic CMOS transistors [12] are fabricated on a polyimide film, and they are covered with a protective layer of parylene. Connection pads to the paper are formed with gold on top of this protective layer. The interconnects are ink-jet printed with a silver nanoparticle ink [29] onto the paper by users. In this UCLP, a 3-mm pad- and via-pitch rule is adopted, and each via extension is 300 μm. The line/space design rule (L/S = 200 μm) of the printed interconnect is determined by both printing resolution and sheet resistance. Typical printers realize 100-μm resolution with the silver nanoparticle ink. However, the minimum line width should be determined by the sheet resistance of the ink. The sheet resistance depends on the room temperature and relative humidity during printing. A sheet resistance of 0.14 Ω/square can be achieved by family use printers at a

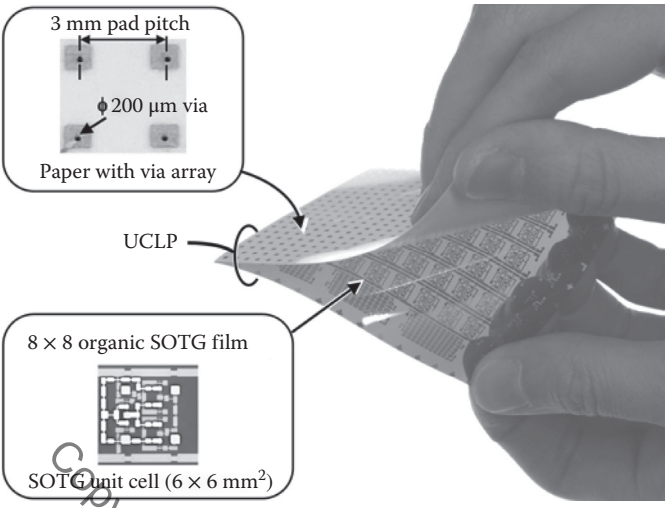


FIGURE 5.3 Prototype of a user customizable logic paper.

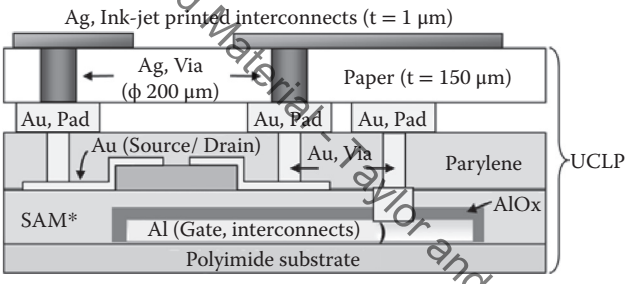


FIGURE 5.4 Cross-sectional view of a user customizable logic paper. (K. Ishida et al., User customizable logic paper (UCLP) with sea-of transmission gates (SOTG) of 2-V organic CMOS and ink-jet printed interconnects, *IEEE Journal of Solid-State Circuits*, 46(1), 285–292, © 2011 IEEE.)

high room temperature of 30°C and relative humidity of 80%. However, we assume a sheet resistance of 0.2 Ω/square by considering a practical room temperature of 17°C and relative humidity of 35%. We adopt 200 μm wide interconnects in this study, and thus resistance between two pads can be estimated around 2.2 Ω. The line space of 200 μm is determined by crosstalk. The crosstalk of the proposed printed interconnects is caused by a resistive coupling rather than a capacitive coupling. The sheet resistance of the precoated nanoconductive base is typically 9×10^9 Ω/square, but satellite ink drops by family use printers lower the actual sheet resistance to around 10% of this value. Thus, the isolation of 20-mm-long interconnects with a space of 200 μm can be estimated at around 9 MΩ. The minimum via-hole diameter should be larger than 200 μm to achieve an acceptable via resistance of 2.7 Ω. Finally, to implement practical circuits, the number of interconnects between the pads should be around five. As a result, a 3-mm pad- and via-pitch rule is determined.

The large pad and via pitch present a design challenge for UCLP to increase integration density. Gate array (G/A) architectures have been widely used in silicon technologies. The G/A architecture includes two pMOS transistors, two nMOS transistors, and nine via holes in a logic cell. In silicon technologies, a narrow via spacing rule is available, and therefore, the number of vias is not critical in the cell area. On the other hand, as a 3-mm pad- and via-pitch are adopted in UCLP, pads and vias now dominate the cell area. The number of vias becomes a critical issue in UCLP, and to solve the problem, an area-efficient SOTG is proposed instead of the conventional G/A approach.

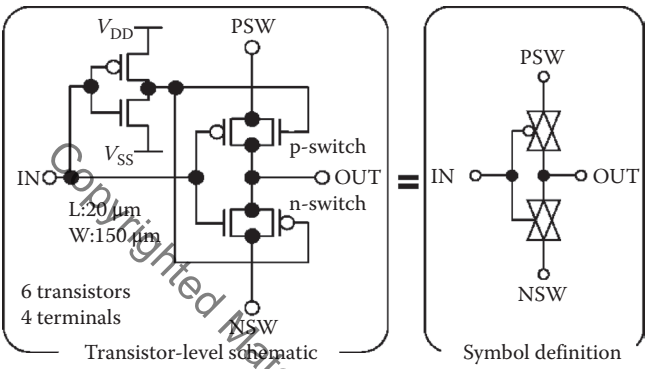
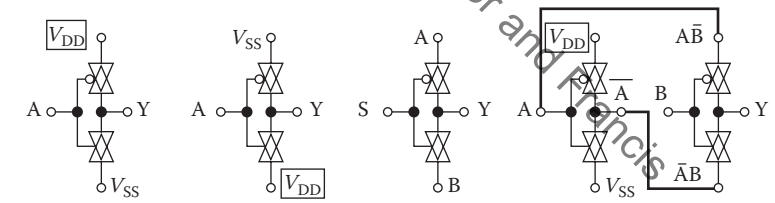
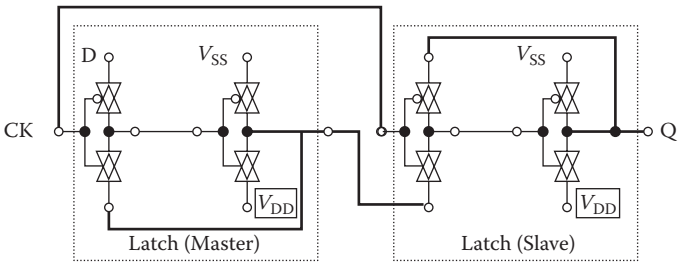


FIGURE 5.5 Schematic and symbol definition of sea-of transmission-gates unit cell. (K. Ishida et al., User customizable logic paper (UCLP) with sea-of transmission-gates (SOTG) of 2-V organic CMOS and ink-jet printed interconnects, *IEEE Journal of Solid-State Circuits*, 46(1), 285–292, © 2011 IEEE.)



(a) Inverter ($Y = \bar{A}$) (b) Buffer ($Y = A$) (c) Multiplexer (d) XOR ($Y = \bar{A}B + A\bar{B}$)



(e) D-flip flop

FIGURE 5.6 Examples of logic gate implementation with sea-of transmission-gates cells. (a) Inverter, (b) buffer, (c) two-input multiplexer, (d) two-input XOR, and (e) D-flip flop.

Figure 5.5 shows the schematic of the SOTG unit cell. SOTG uses a type of pass transistor logic, and a single SOTG cell has six transistors. Each unit cell has a pair of complementary transmission gates, n-switch (NSW) and p-switch (PSW), and four terminals for ink-jet printed interconnects. V_{DD} and V_{SS} are common to every SOTG cell. In SOTG, the output (OUT) is connected to either PSW or NSW depending on the input (IN). Figure 5.6 shows several examples of basic logic gate implementation with the proposed SOTG cells. An inverter requires one logic cell that consists of six transistors, as shown in Figure 5.6a. In terms of saving on rewiring cost or area, the SOTG architecture makes it easy to customize the UCLP. In fact, either a buffer or a two-input multiplexer can be implemented with one logic cell, as shown in Figure 5.6b and c. Thanks to the complementary transmission gates, not only the XOR as shown in Figure 5.6d but also any two-input logical operation can be realized with two logic cells. In addition, a D-flip flop can be implemented with only four logic cells as shown in Figure 5.6e. A total of 64 logic cells are implemented in 73×73 mm^2 area.

5.3.3 Insole Pedometer with Piezoelectric Energy Harvester

Energy harvesting is an enabling technology for realizing an ambient power supply for wireless sensor nodes and mobile devices. By using flexible photovoltaic cells and piezoelectric films, we can readily harvest ambient energy if flexible energy harvesters can be realized. Conventional silicon circuits, however, are not best suited to realizing flexible large-area energy harvesters because they are not mechanically conformable to uneven surfaces such as shoes. To address this challenge, an organic insole pedometer with a piezoelectric energy harvester is proposed as the first step toward ambient energy harvesting using organic flexible electronics [20].

The main challenge in the design of organic circuits for piezoelectric energy harvesting is the robust operation of pMOS-only circuits at a low-supply voltage. In energy-harvesting applications, the harvested power is small and the rectified voltage is low (e.g., 2 V). In organic circuit design, pMOS-only circuits are often used, because the mobility of pMOS transistors is much higher than that of nMOS transistors in our process. The operation of pMOS-only circuits is not robust, and the noise margin is small because of their rationed-logic nature. A pseudo-CMOS inverter that consists of four pMOS transistors [30] has a high gain, but it requires a negative voltage bias. In energy-harvesting applications, however, a single power supply is typical. Therefore, in this work, to increase the noise margin of pMOS-only logic circuits, a negative voltage is generated by a charge pump and is applied as the bias of pseudo-CMOS inverters. We use a 2 V pMOS process with SAM technology [12] and dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNTT) [31] for pMOS transistors.

Figure 5.7 shows the photograph of the prototype insole pedometer that includes the piezoelectric energy harvester and the 2 V organic pMOS rectifier and counter. A polyvinylidene difluoride (PVDF) sheet is used as the piezoelectric energy harvester. Twenty-one rolls of PVDF film are embedded in the insole. Each time the insole is pressed by the foot during walking, the harvested energy is rectified by the organic rectifier, and the number of the steps is counted by the organic counter. Figure 5.8 shows a block diagram of the proposed organic insole pedometer. It consists of four circuit blocks. The all-pMOS full-wave rectifier supplies a voltage V_{DD}

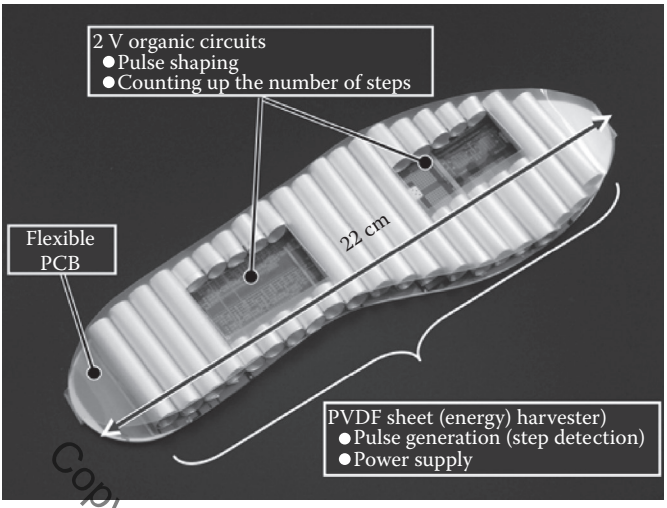


FIGURE 5.7 Photograph of the prototype insole pedometer.

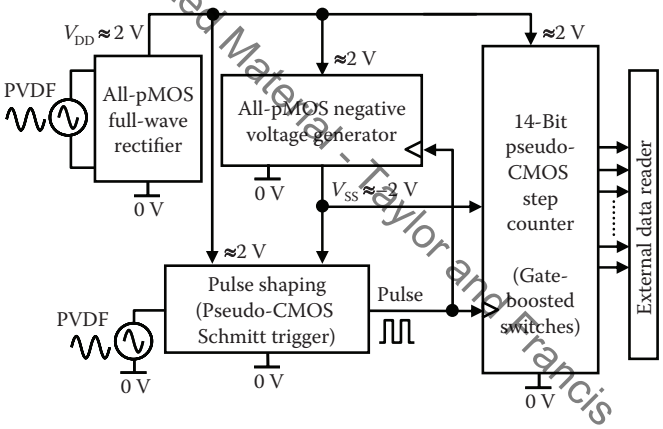


FIGURE 5.8 Block diagram of the insole pedometer. (K. Ishida et al., Insole pedometer with piezoelectric energy harvester and 2 V organic circuits, *IEEE Journal of Solid-State Circuits*, 48(1), 255–264, © 2013 IEEE.)

of approximately 2 V to all circuit blocks. In the clock generator, the output of the PVDF harvester is half-wave-rectified and a Schmitt trigger inverter converts the half-wave-rectified signal into a clock signal. The generated clock signal is sent to both the pMOS negative voltage generator and the 14-bit pseudo-CMOS step counter with gate-boosted pMOS switches. The step counter records the number of steps up to 16,383 steps at the maximum frequency of 4.4 Hz using the harvested power. The negative voltage generator supplies a voltage V_{SS} (e.g., −2 V) to the counter and can provide 12 μW power with 65% efficiency. The organic insole pedometer consists of 462 transistors, and its size is 22×7 cm^2.

5.3.4 100 V AC Energy Meter

A smart meter is essential for realizing the power grid. To reduce the energy loss in the power grid, an extremely fine-grain power monitoring system is desirable, and it will require an enormous number of low-cost power meters. Existing power meters, however, do not meet the cost and size requirements. On the other hand, organic devices on flexible films have a great potential to realize low-cost power meters. In this context, a 100 V AC power meter based on a system-on-a-film (SoF) concept is presented in Ishida et al. [21].

Figure 5.9 shows the photograph of the proposed 100 V AC power meter on a flexible film, including (1) analog circuits composed of a 20 V organic CMOS opamp for AC current sensing, (2) logic circuits composed of a 20 V organic CMOS frequency divider for integrating the measured current, (3) AC-to-DC power converter composed of a 100 V organic pMOS rectifier to generate 20 V DC power for the power meter, (4) an organic light-emitting diode (OLED) [32] bar indicator, and (5) an AC connector inserted between the power plug and the AC outlet are fully integrated on a 200 × 200 mm^2 flexible film. The entire sheet can be folded, and the total size of the proposed AC power meter can be shrunk to 70 × 70 mm^2. Figure 5.10 shows the block diagram of the proposed 100 V AC power meter. The measured 100 V 50 Hz AC load current i_L is first converted into the sense voltage (v) by means of the sense resistor (R). The converted sense voltage v is then amplified by the amplifier and rectified into V_{SENSE}, which is compared with the triangular waveform (V_{TRI}) by the comparator. The output of the comparator enables or disables the 10-bit counter. Five most significant bits in the counter are connected to the OLED bar indicator.

To get the accumulated results, the maximum integration time of the power meter is designed to be 43 minutes. The 0.05 Hz clock for the input of the triangular

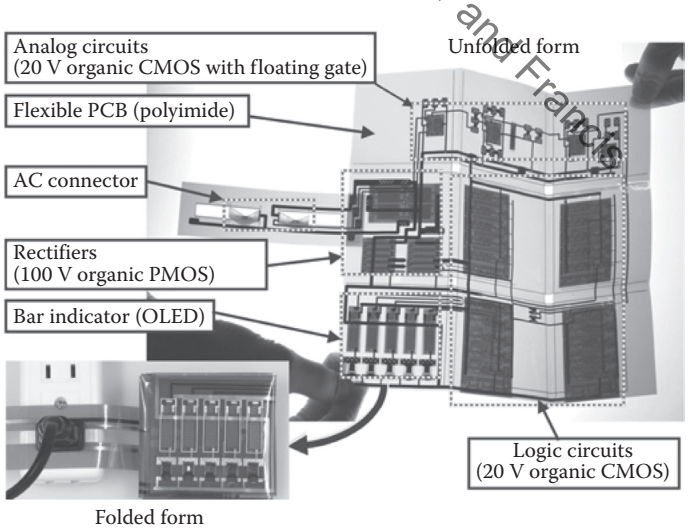


FIGURE 5.9 Prototype of the organic 100 V AC energy meter on a flexible film. (K. Ishida et al., A 100 V AC energy meter integrating 20 V organic CMOS digital and analog circuits with a floating gate for process variation compensation and a 100 V organic PMOS rectifier, *IEEE Journal of Solid-State Circuits*, 47(1), 301–309, © 2012 IEEE.)

waveform generator and the 0.4 Hz clock for the counter are generated by a 10-bit frequency divider, for which the clock is generated by a half-wave rectifier from 100 V 50 Hz AC signal. The required DC power for the power meter is provided by converting the 100 V 50 Hz AC power into 20 V DC power by the full-wave rectifier implemented using 100 V organic pMOS. The current consumption of the system, mainly consumed by the five-digit OLED bar indicator, is around 2 mA. As the driving capability of organic nMOS is weaker than that of pMOS by an order, an all-pMOS full-wave rectifier topology is chosen. The gate length and width of each transistor are 20 μm and 100 mm, respectively, which can supply up to 2 W DC power, the highest power level ever reported.

In our 20 V CMOS, DNTT-based pMOS transistor has eight times higher carrier mobility than that of Naphthalenetetracarboxylic diimide-based nMOS. In addition, our CMOS inverter gain was only 3.2 at 20 V and this leads to functional errors in the large-scale logic circuits. To solve the problem, we designed the frequency divider with high-gain pseudo-CMOS inverters [30]. The pseudo-CMOS inverter uses only pMOS. The gain of 148, static noise margin of 6.7 V, and 156-Hz oscillation frequency of a three-stage ring oscillator can be achieved at 20 V supply voltage. In the divider, nMOSs are still used only for transmission gates, in which high gain is not required. Thanks to the high gain of pseudo-CMOS, the divider successfully operates at 50 Hz and 20 V. In the frequency divider, the dynamic slave latch, which consists of only an inverter and the parasitic capacitance as the charge keeper, is used to reduce the number of transistors.

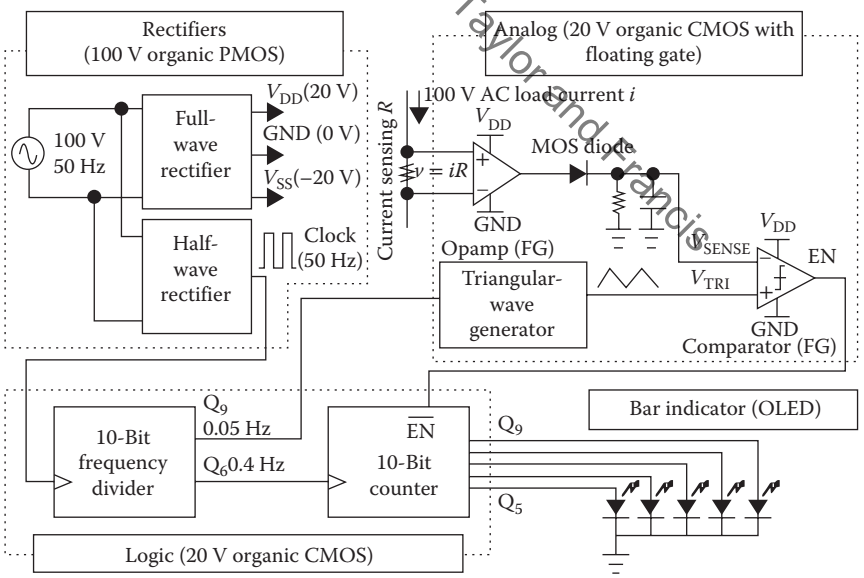


FIGURE 5.10 Block diagram of the AC energy meter. (K. Ishida et al., A 100 V AC energy meter integrating 20 V organic CMOS digital and analog circuits with a floating gate for process variation compensation and a 100 V organic PMOS rectifier, *IEEE Journal of Solid-State Circuits*, 47(1), 301–309, © 2012 IEEE.)

A major challenge in organic analog circuit design is to compensate for large process variations. The offset voltage in the differential pair of the amplifier due to the device mismatch should be reduced to lower than the sense voltage generated by the sense resistor R in Figure 5.10. The AC energy meter consists of 609 transistors and the total area excluding AC connector is 200×200 mm^2 (unfolded form) or 70×70 mm^2 (using form).

5.4 CONCLUSIONS

In this chapter, resent progress of organic transistors and their circuit blocks are briefly surveyed. The improvement of the organic technologies enables the implementation of highly integrated circuit blocks such as microprocessors and ADCs on a flexible film. Self-assembled monolayer technology drastically lowers the operation voltage of organic transistors down to 1 V. Fully printed technology will reduce the total cost of the large-area electronics in the near future.

Some feasibility studies of the organic flexible applications are also introduced. The EMI measurement sheet, the UCLP, and the insole pedometer utilize the advantage of 2 V organic transistors. In particular, the direct silicon-organic circuit interface will bring more possibilities of new application. In contrast, the 100 V AC energy meter employs 20–100 V organic transistor. The drawback, that the device requires high-voltage power supply, turns to an advantage because the energy meter should handle high voltages. As previously mentioned, flexible electronics with organic transistors will open up new application fields.

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