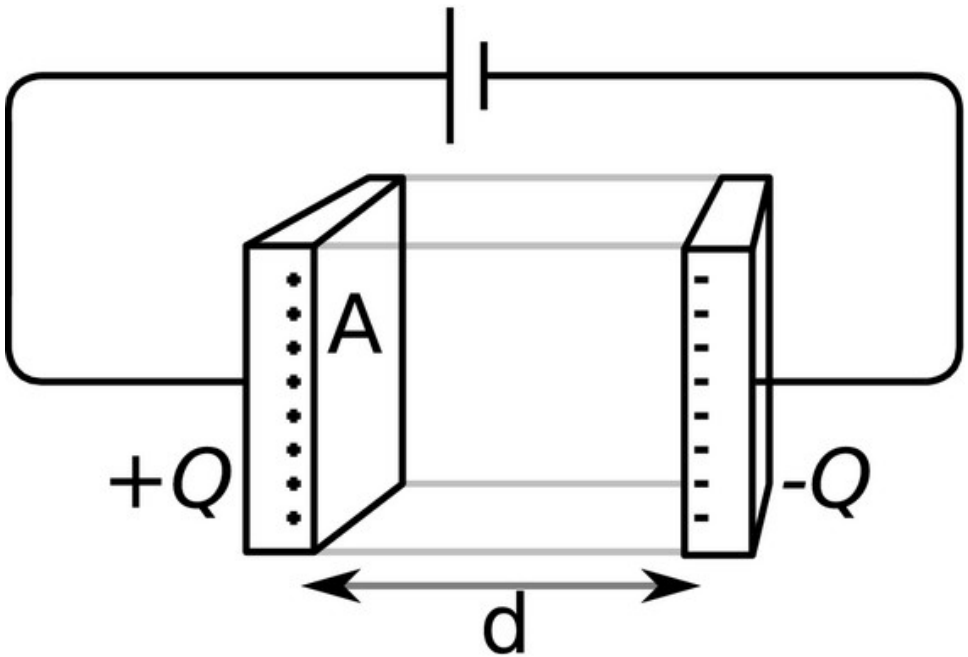

Figure 11.1 The capacitor structure. When a voltage is applied, charge *Q* is accumulated on the electrodes at the interface with the insulating material.

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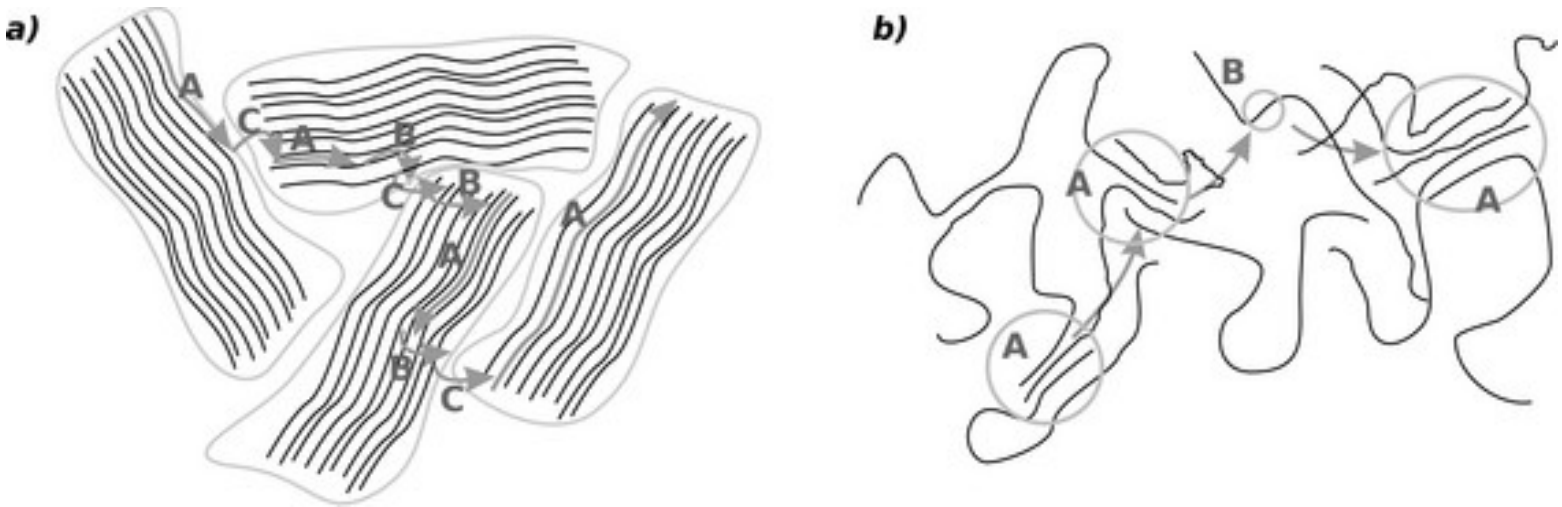

Figure 11.2 (a) The hopping transport mechanism principle in a conductivity network. Intra-chain transport is indicated with A, B represents interchain transport, and C indicates transport between different ordered domains. The arrows show the path of the charge carrier through the material. (b) Hopping transport through ordered domains A and single hopping sites B in a disordered material with small amount of ordered domains in an amorphous matrix, which is typically the case in a polymeric material.

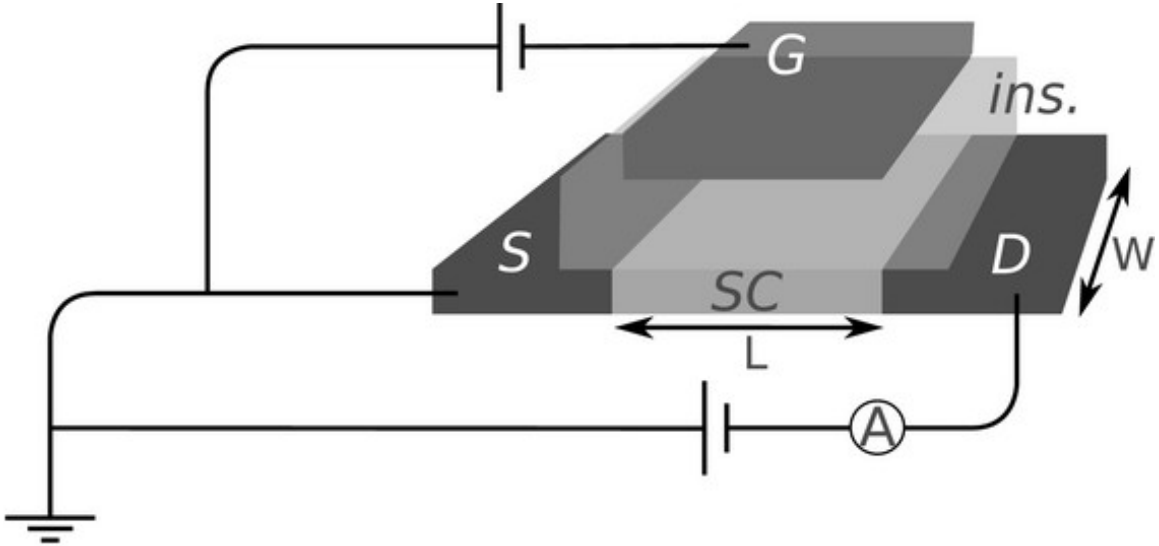

Figure 11.3 Typical device structure of an organic thin-fi lm transistor (TFT) (in the so-called top-gate configuration, the gate electrode layer is applied last) in a measurement circuit, the output characteristics are measured as the drain current as a function of drain voltage at different gate voltages. In a real measurement, the current is measured on all three terminals of the device. The transistor channel region dimensions are marked *W* (width) and *L* (length). Usually, the width is much larger than the length of the channel region.

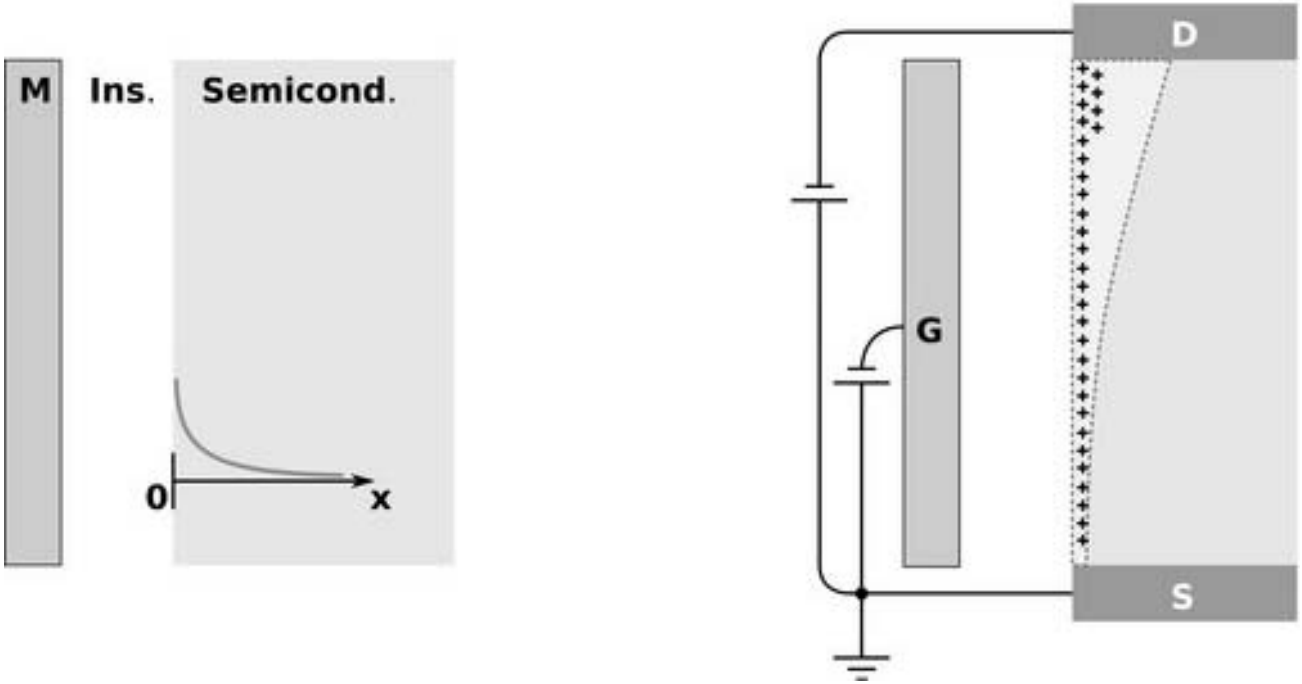

Figure 11.4 Schematic drawing of a metal–oxide–semiconductor (MOS) capacitor and the corresponding field-effect transistor (FET) circuit used for modelling the metal–insulator–semiconductor field-effect transistor (MISFET) structure. The area marked “M” is the metallic gate electrode and the gray area is the semiconductor separated by an insulating layer. The *x*-axis shows the distance from the insulator–semiconductor interface into the bulk of the semiconductor and the gray curve indicates a induced charge carrier distribution (left). The lightened area of the semiconductor (right) schematically shows the accumulated charge carrier (+) region.

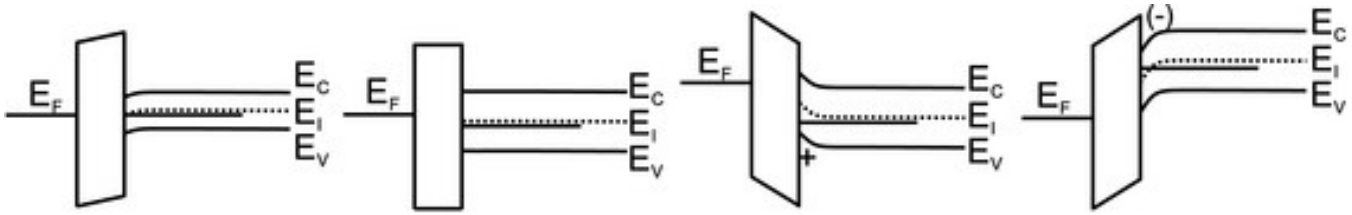

Figure 11.5 Different biasing regions for a p-type device showing the energy diagrams at *V*G = 0 V, under flat-band, in accumulation and under depletion conditions (from left to right). Flat-band condition corresponds to a bias resulting in no band-bending in the semiconductor. In an ideal device, flat-band appears at *V*G = 0 V. For details see, for example, Refs. [42,43]. The energy level indices are F = fermi, C = conduction, V = valence, and I = intrinsic.

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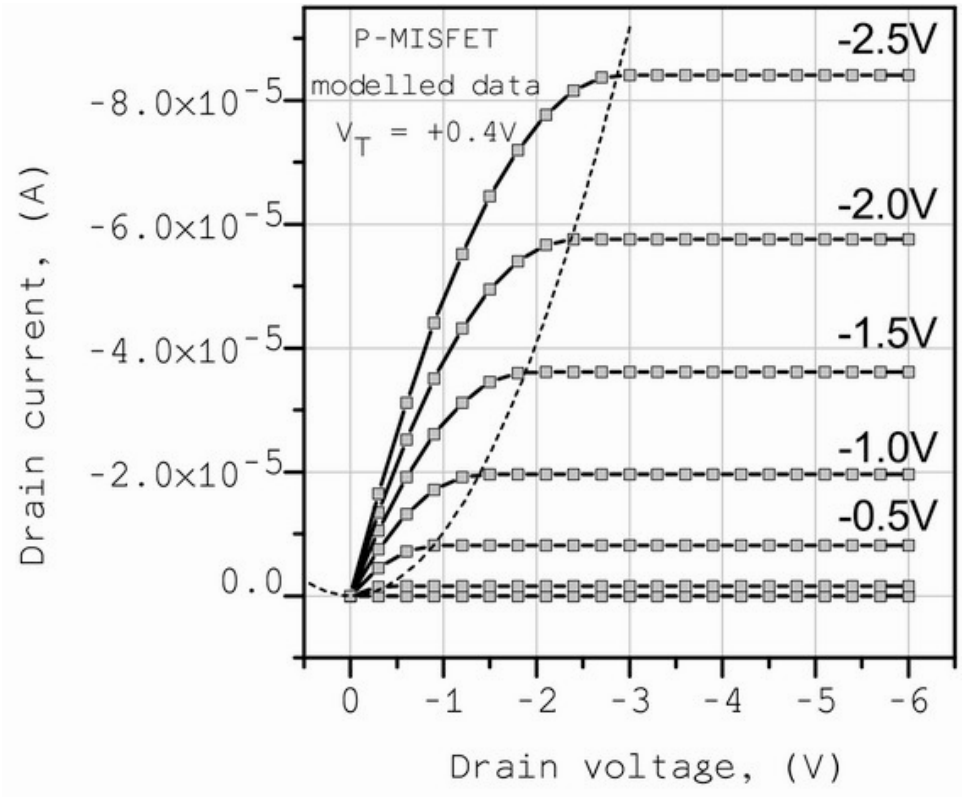

Figure 11.6 Typical output characteristics for a p-type metal–insulator–semiconductor field-effect transistor (MISFET).

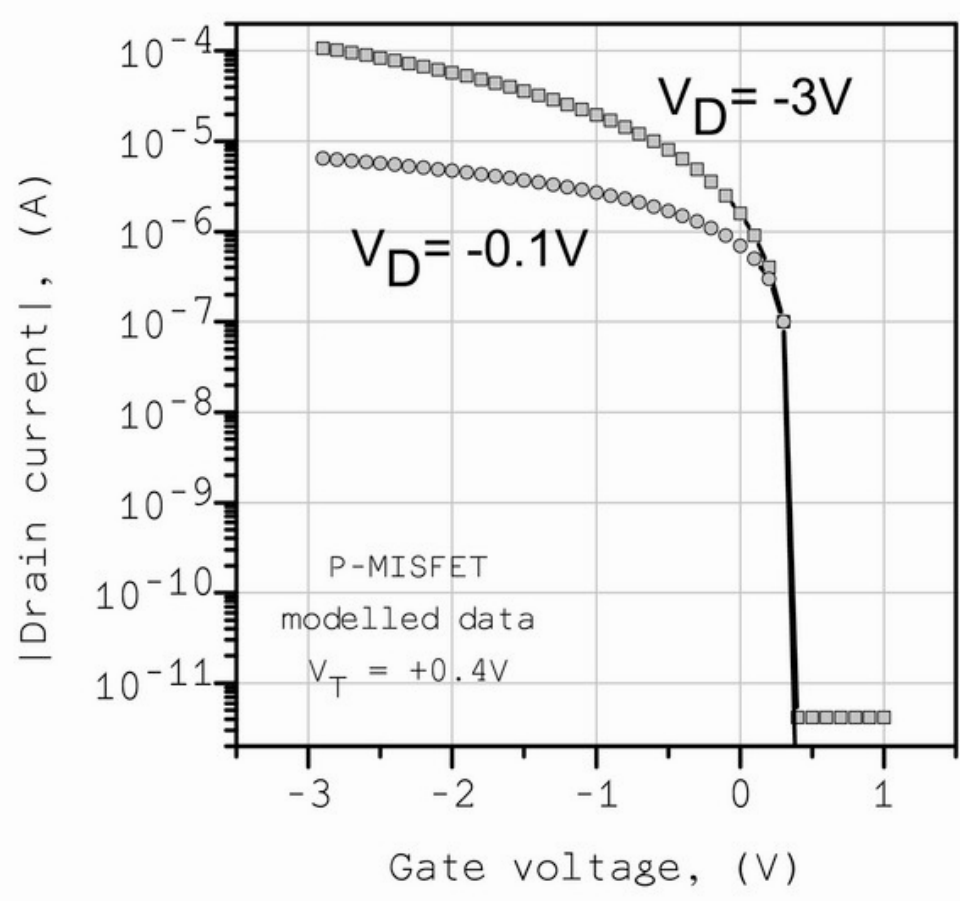

Figure 11.7 Typical transfer curve for a p-type metal–insulator–semiconductor field-effect transistor (MISFET).

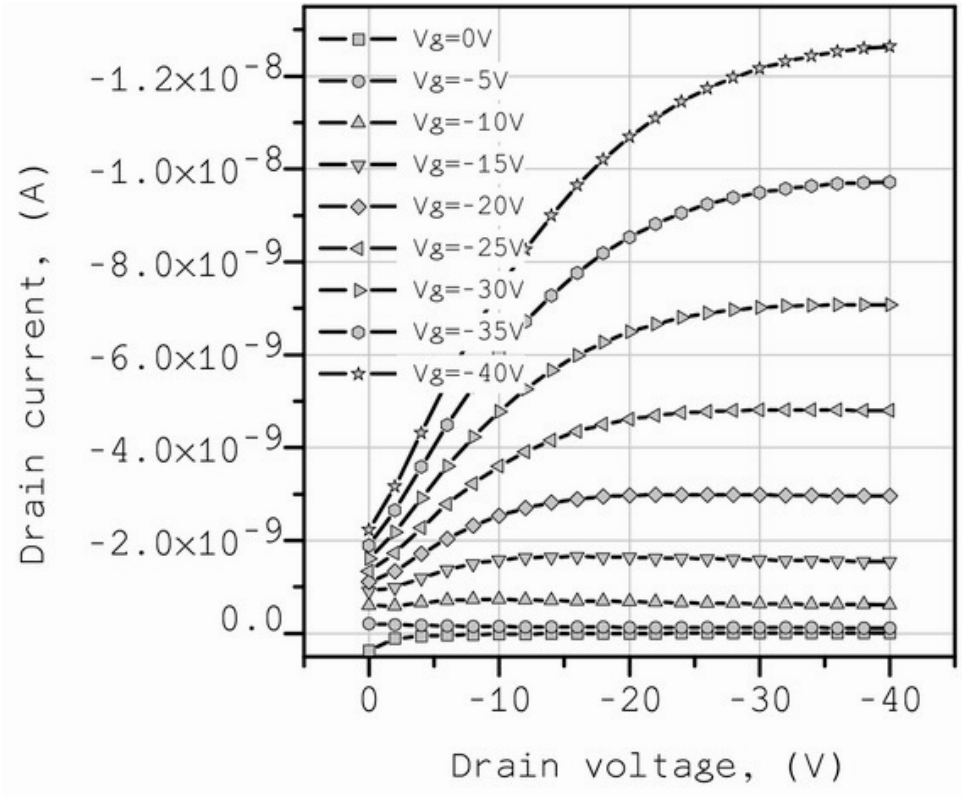

Figure 11.8 Typical polymer field-effect transistor (FET) output curves. The following are the typical discrepancies shown: (a) the transition from the linear to the saturated regime is very smooth, (b) there is an offset between the *I*–*V* curves at low field proportional to the gate leakage, and (c) the *I*–*V* curves tails off toward origin, testimony of nonideal contacts between semiconductor and source–drain contacts.

Figure 11.9 Schematic drawing of the spin coating process. The material is deposited in solution and the substrate is then rotated to flatten the drop of liquid while it dries out.

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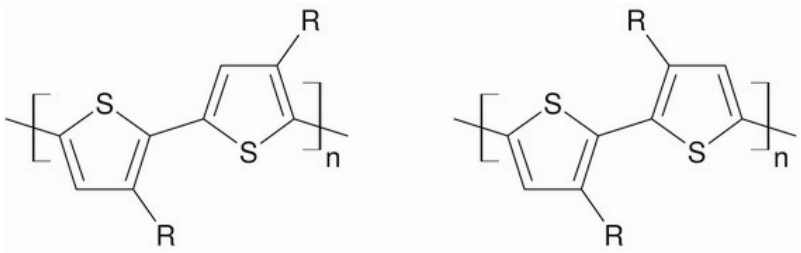

Figure 11.10 The chemical structure of RR-P3HT with the side chain always attached to the same position on the thiophene ring (left). In a regiorandom poly(3-hexylthiophene), the side chains are randomly attached to each other in a head-to-head or head-to-tail configuration.

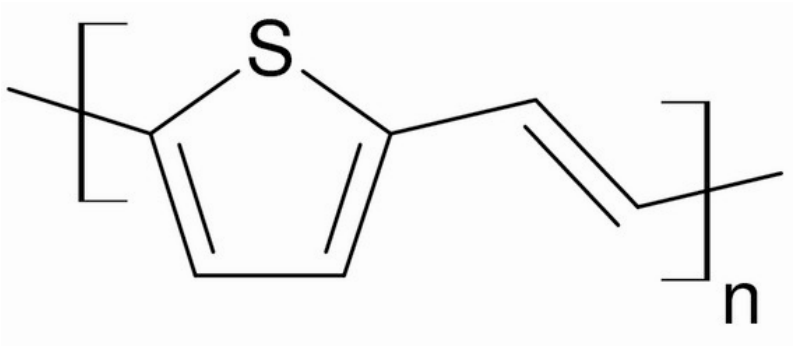

Figure 11.11 The chemical structure of poly(thienylene vinylene) (PTV).

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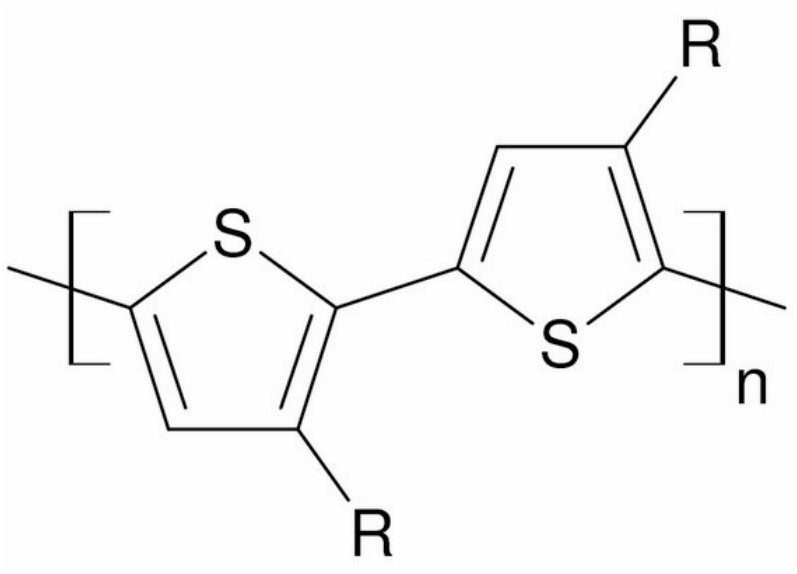

Figure 11.12 Chemical structure of RR-P3HT where the side chain R is a regular hexyl chain.

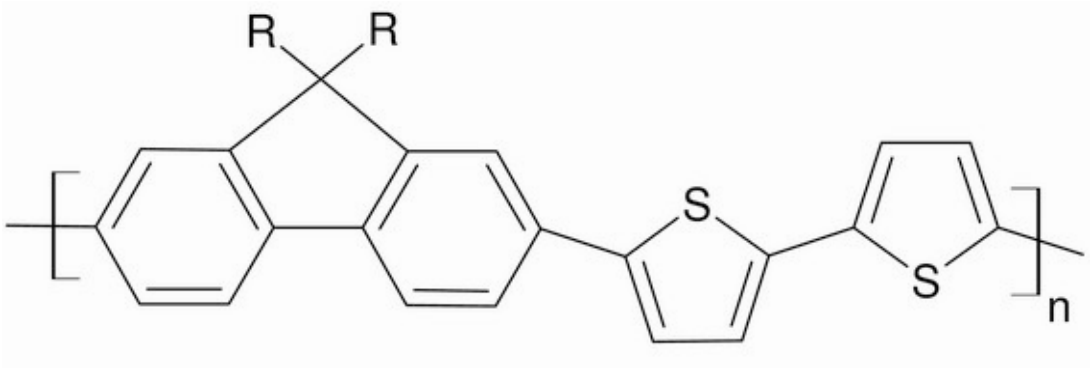

Figure 11.13 Chemical structure of F8T2. The side chains R = C8H15.

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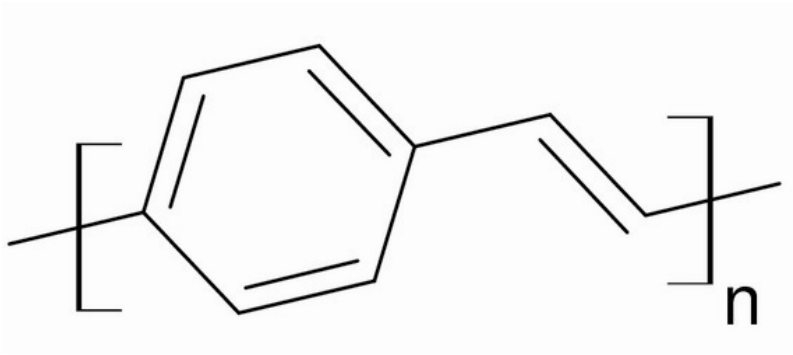

Figure 11.14 The chemical structure of poly(*p*-phenylene vinylene).

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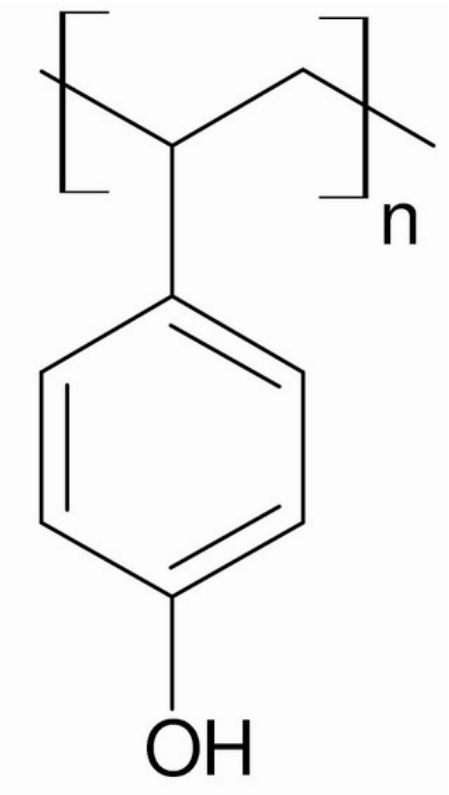

Figure 11.15 Structure of polyvinylphenol (PVP).

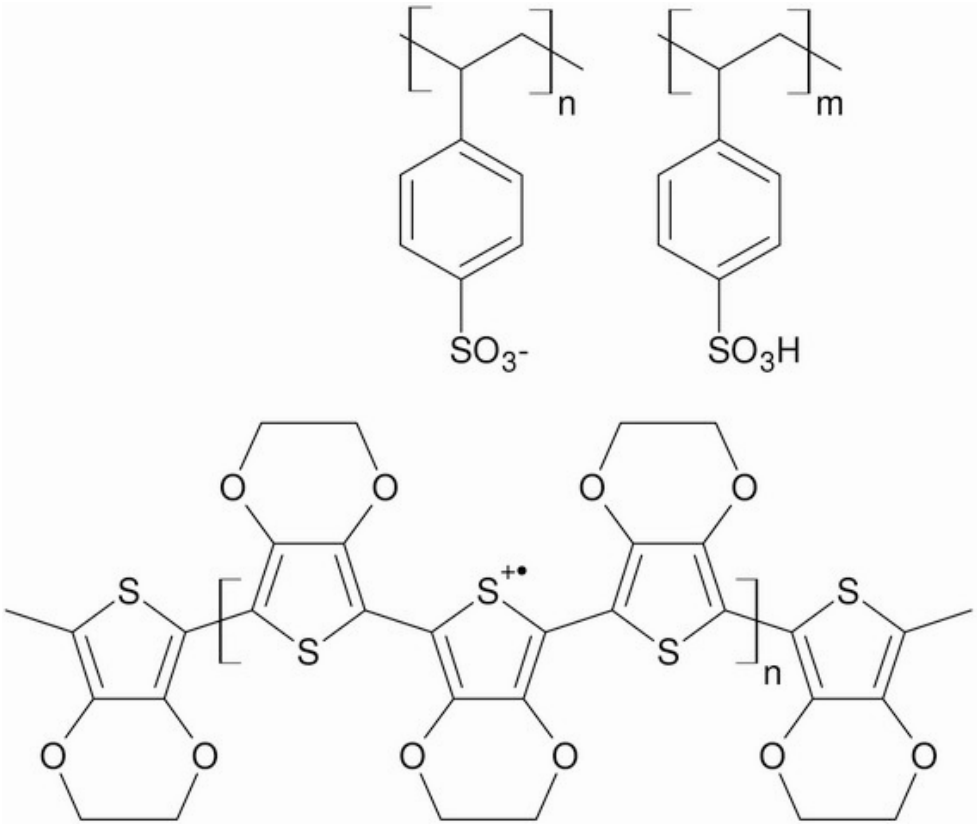

Figure 11.16 Structure of PEDOT:PSS. The acid is a strong dopant for the conjugated polymer resulting in a highly conductive material.

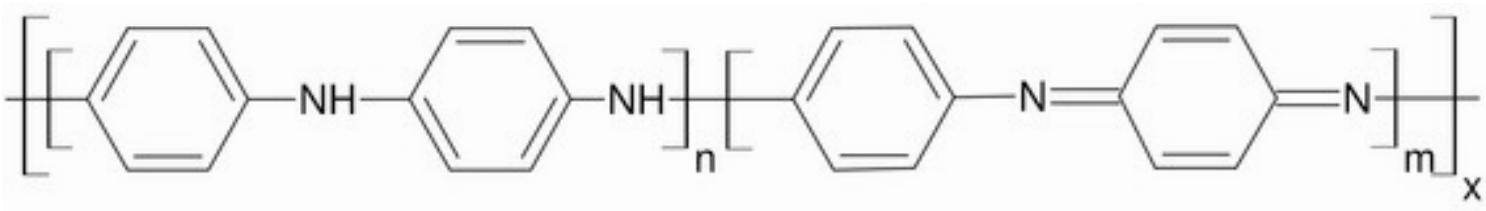

Figure 11.17 Chemical structure of polyaniline (PANI). The different stable oxidation states have different proportions of *n* and *m*.

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Answer to exercise question 2:

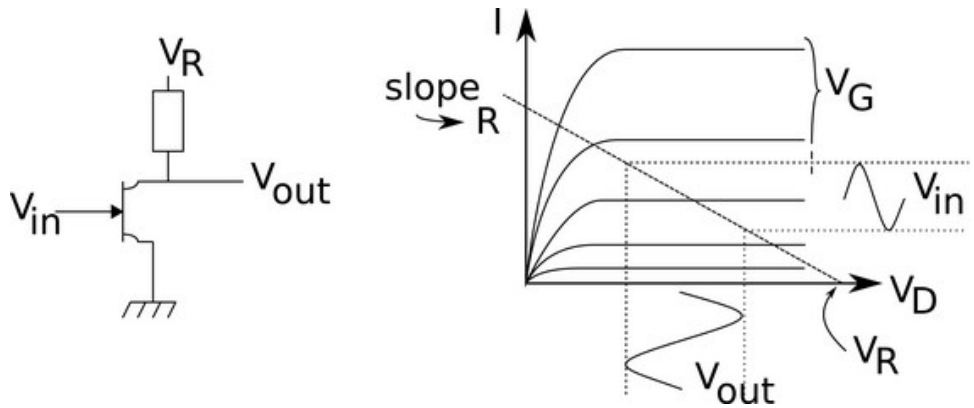

Figure 11.exc2 The most simple amplifier circuit consists of one transistor and a resistor, R, connected to the drain of the transistor. The in-signal, *Vin*, is connected to the gate, and a drive voltage, *VR*, is fed to the other contact of the resistor. The out-signal, *Vout*, is read at the drain while the source is connected to ground. the Gain of the amplifier is directly determined by the transconductance of the device. If the transconductance is greater than one the Gain will be positive (>1) and we will see amplification of the signal. The transconductance is easily estimated from the I-V characteristics. The magnitude of the Gain is further determined by the resistor R and the drive voltage, *VR*.
The relation between gain and the transistor output characteristics may be visualized by the graph below. The "position" and slope of the straight line (*VR* and *R*) must be chosen so that *Vin* does not exceed the saturated region of the I-V curve.