Verilog HDL: Digital Design and Modeling

Chapter 7

Dataflow Modeling

Additional Figures
Figure 7.5  Karnaugh map for a logic circuit to be implemented using continuous assignment statements.

Figure 7.6  Karnaugh map for a circuit to be implemented using continuous assignment statements.
Figure 7.17  Octal-to-binary encoder.

Table 7.2  Truth Table for an Octal-to-Binary Encoder

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<th>Inputs</th>
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Figure 7.18  Logic diagram for an 8:3 encoder.
Figure 7.35  Block diagram of a 4-bit adder to be implemented as a carry look-ahead adder.
Figure 7.40  General block diagram of a fundamental-mode asynchronous sequential machine.

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