Figure 3.1  Bidirectional gates.

Figure 3.11  Three-state gates: bufif0, bufif1, notif0, and notif1.
Figure 3.13  A logic diagram showing single-wire nets and one multiple-wire net, where the connectivity of the logic gates is determined by nets.

Figure 3.18  Wired AND function using two open collector AND gates.

Figure 3.19  Wired OR circuits: (a) using TTL gates and (b) using ECL gates.