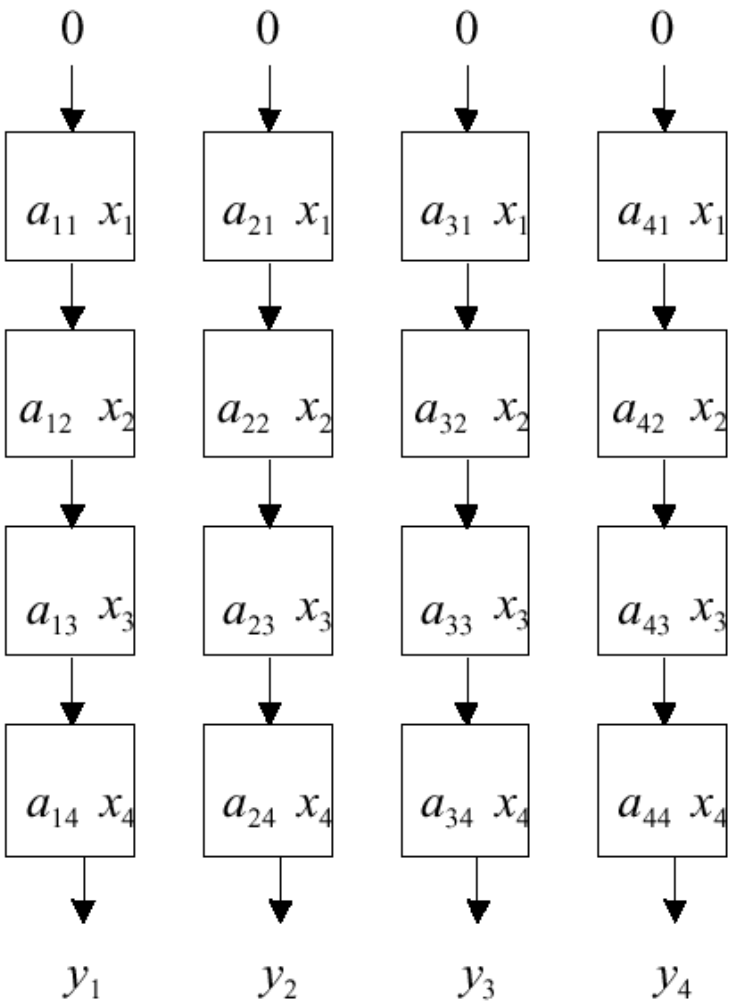
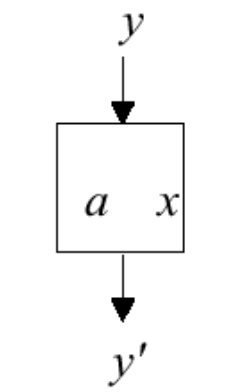
Chapter 12

Array Processors

Multiple Pipeline Structure





$$y' = y + ax$$

Fig. 12.1 Multiple pipeline structure for matrix-vector multiplication.

Array Processor

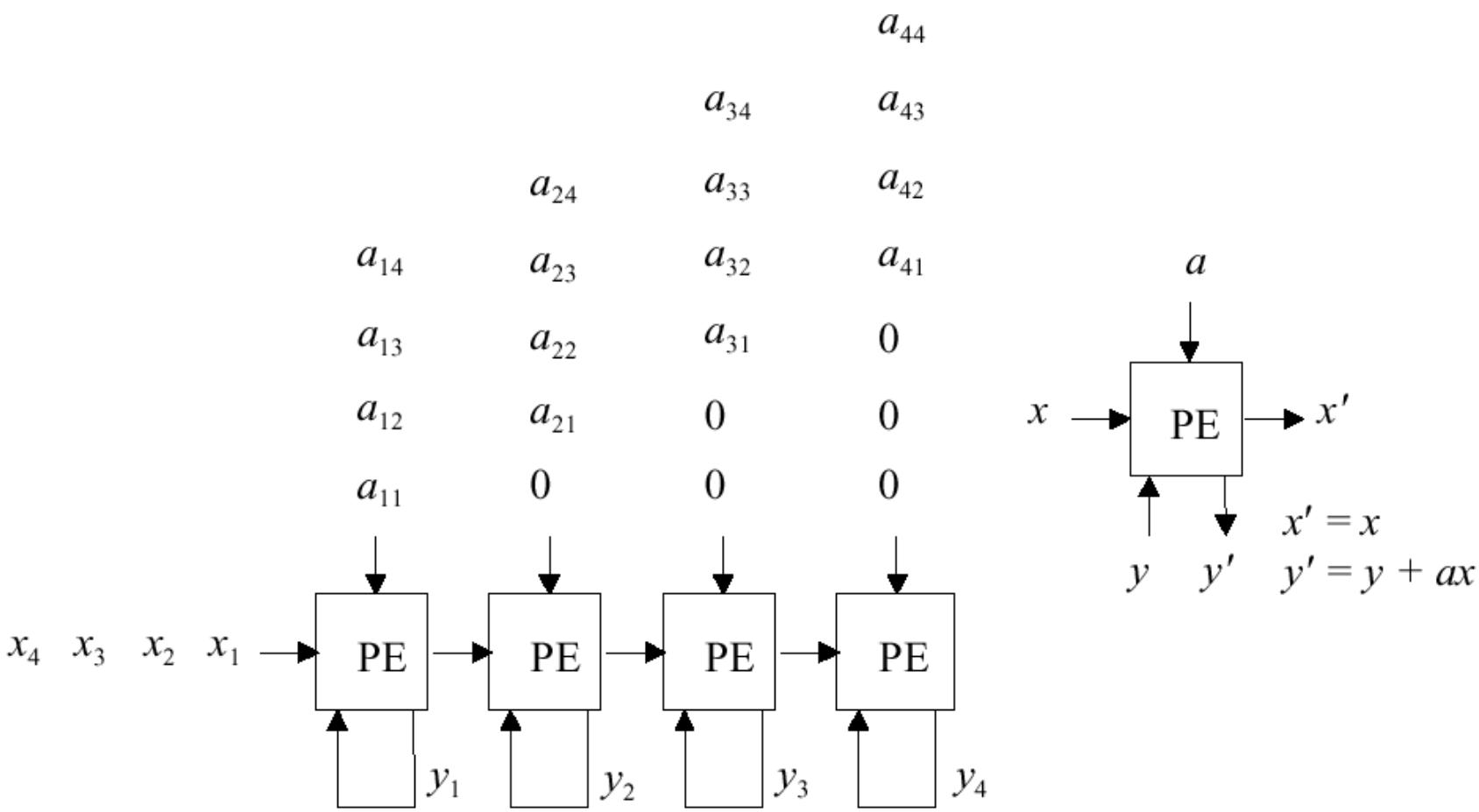


Fig. 12.2 Array processor for matrix-vector multiplication.

Array Processor

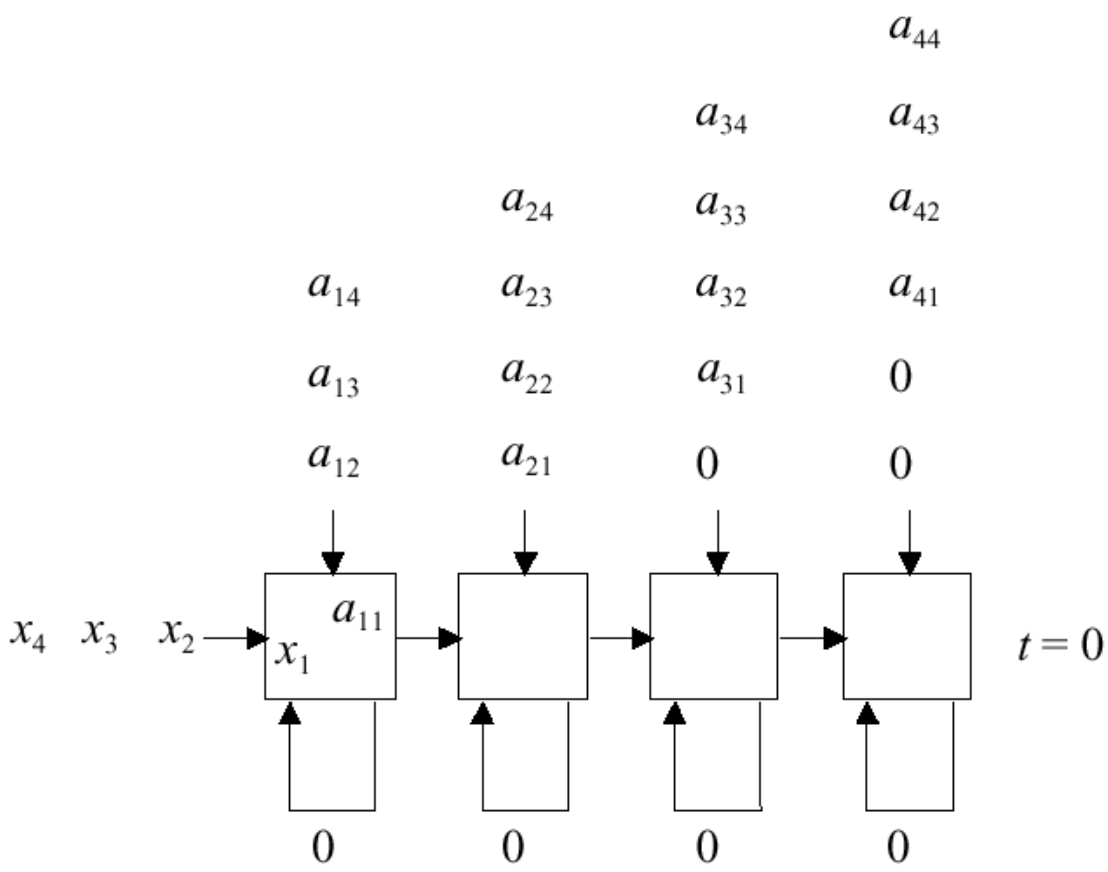


Fig. 12.3 Snapshot of the array processor at $t = 0$.

Array Processor

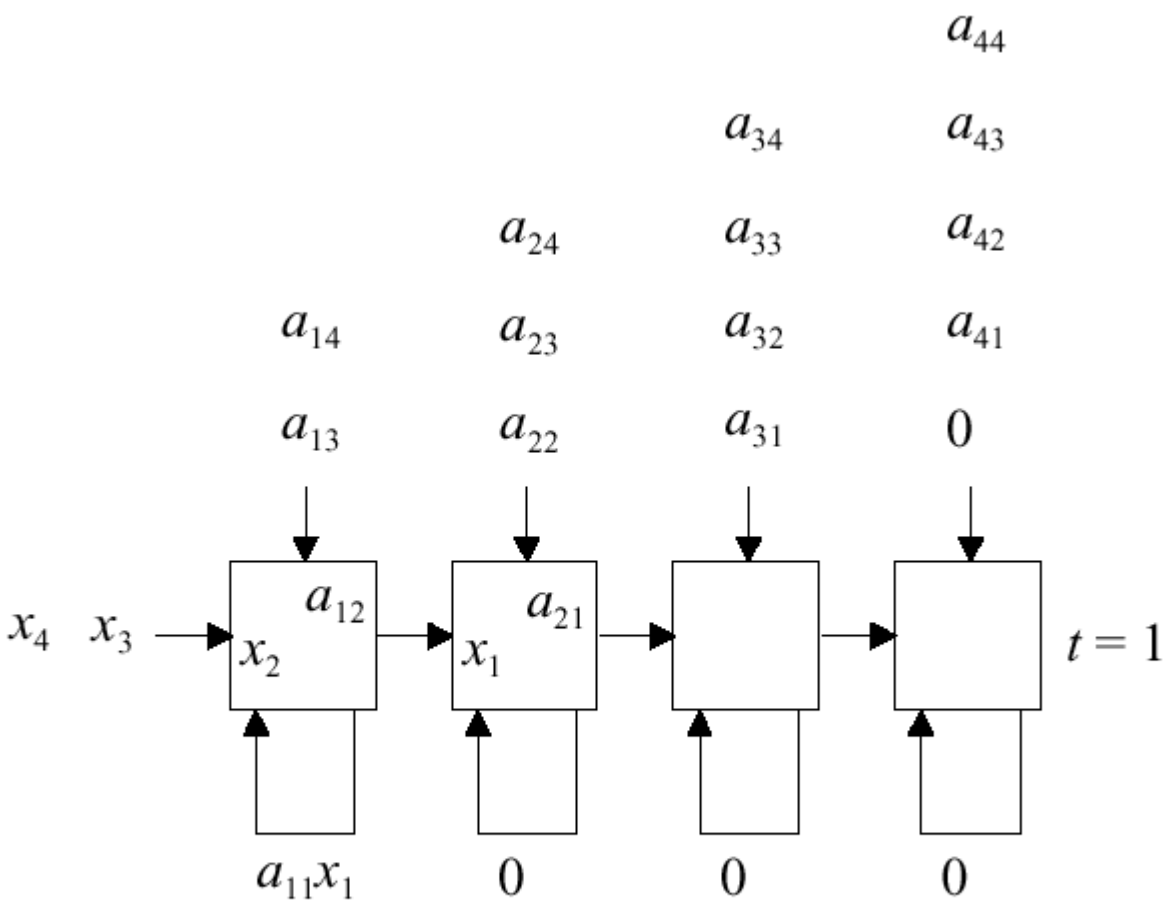


Fig. 12.4 Snapshot of the array processor at $t = 1$.

Array Processor

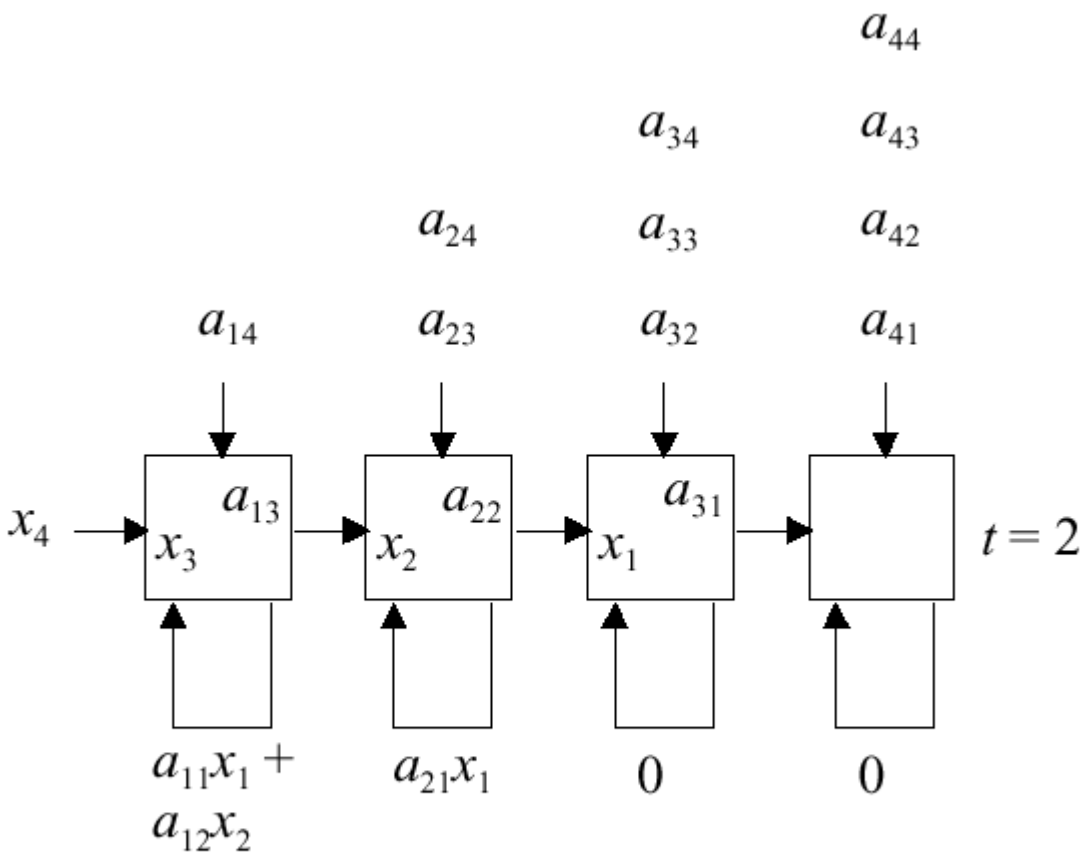


Fig. 12.5 Snapshot of the array processor at $t = 2$.

Array Processor

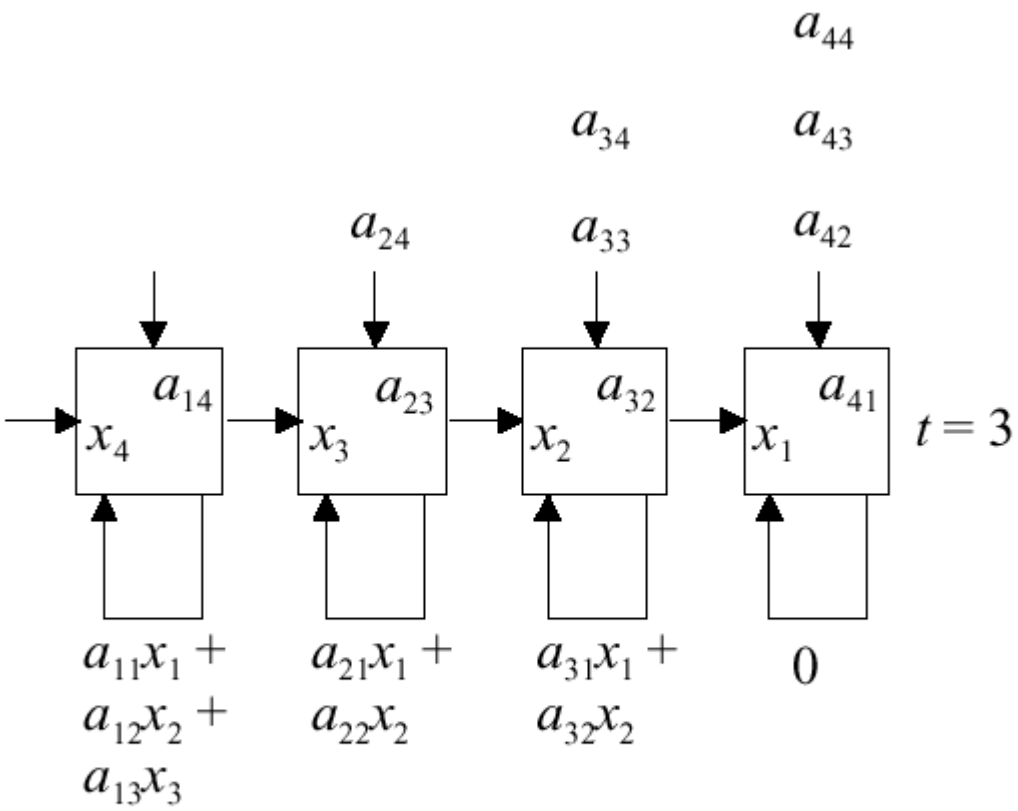


Fig. 12.6 Snapshot of the array processor at $t = 3$.

Array Processor

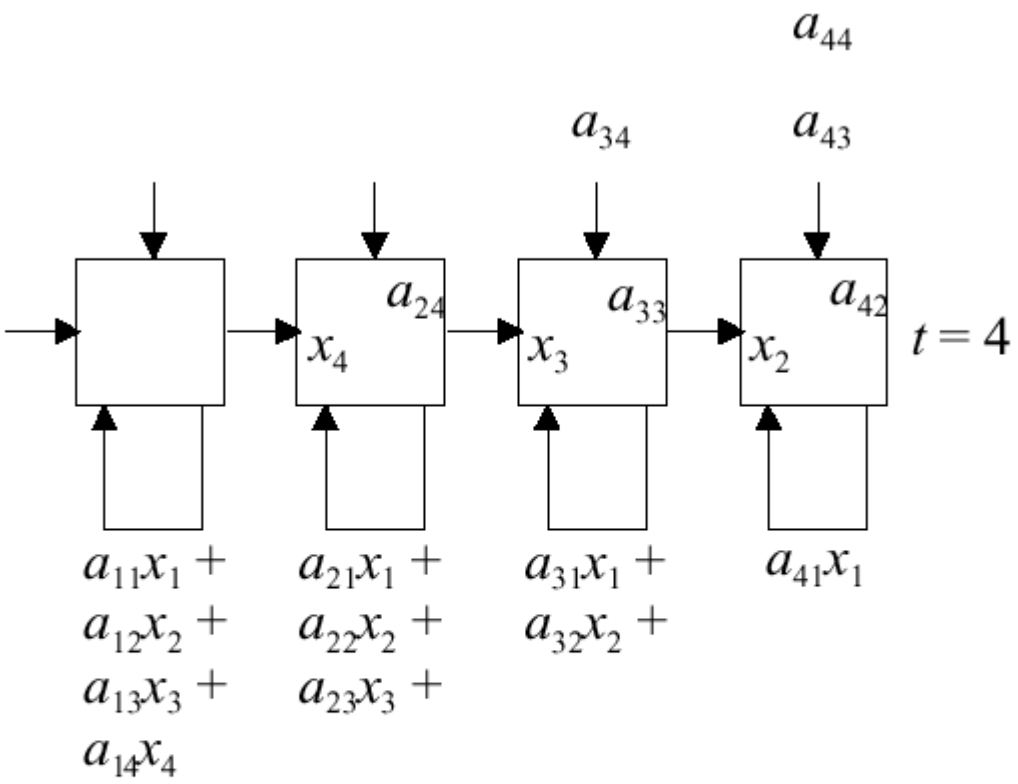


Fig. 12.7 Snapshot of the array processor at $t = 4$.

Linear Array Processor

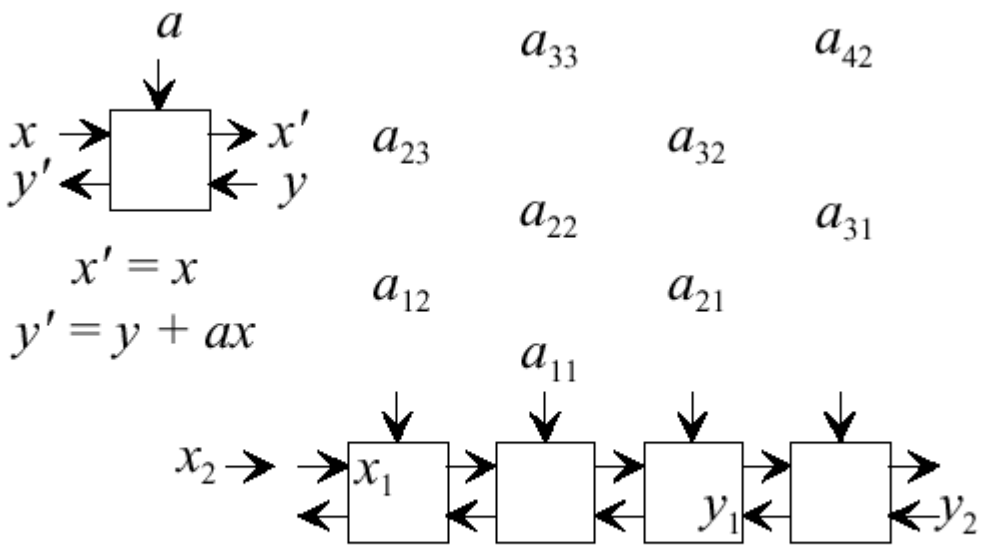


Fig. 12.8 Linear array processor for matrix-vector multiplication.

Array Processor

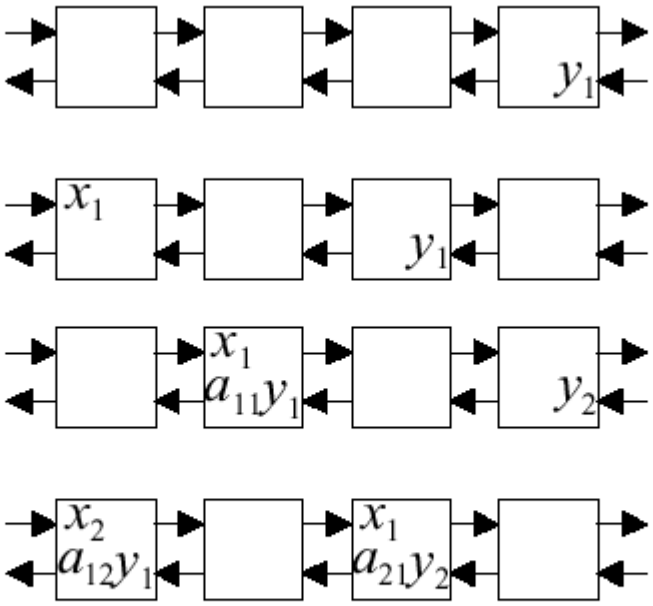


Fig. 12.9 Snapshots of the array processor shown in Fig. 12.8.

Dependence Graph

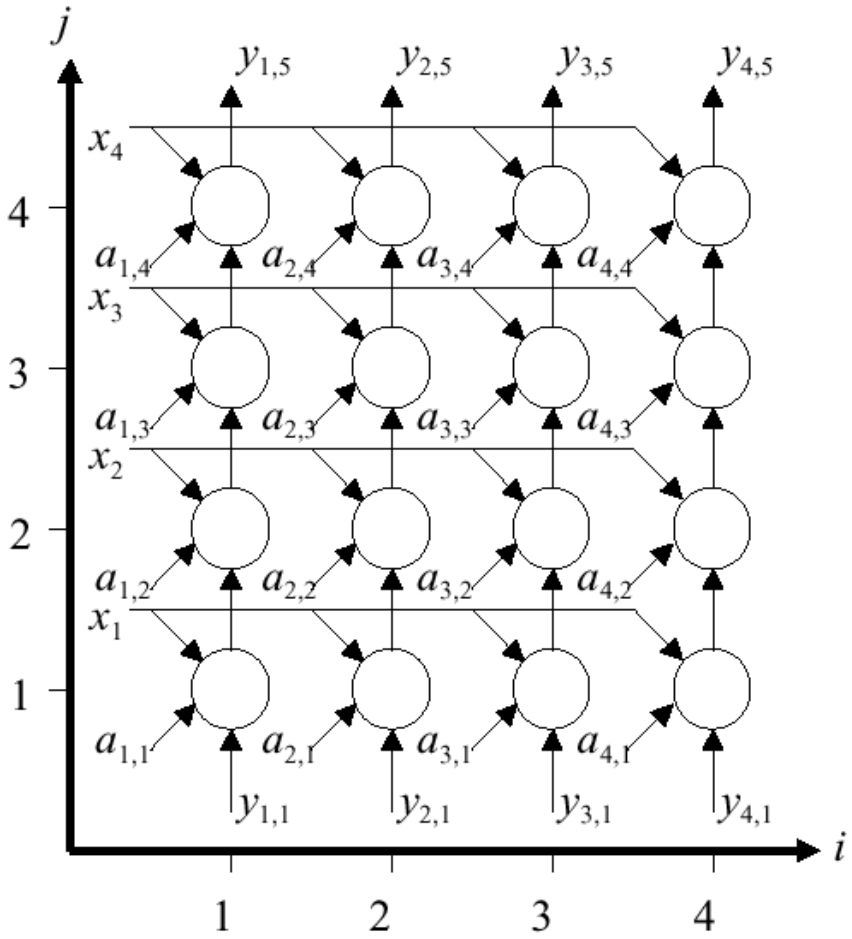


Fig. 12.10 Dependence graph for matrix-vector multiplication.

Dependence Graph

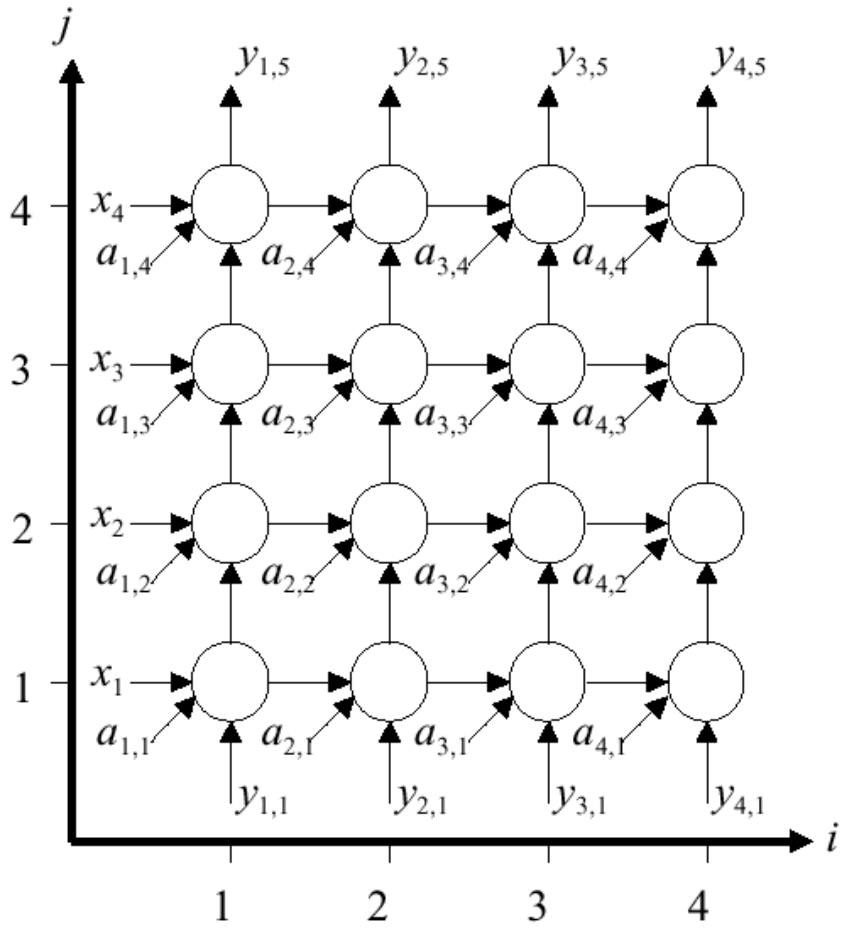
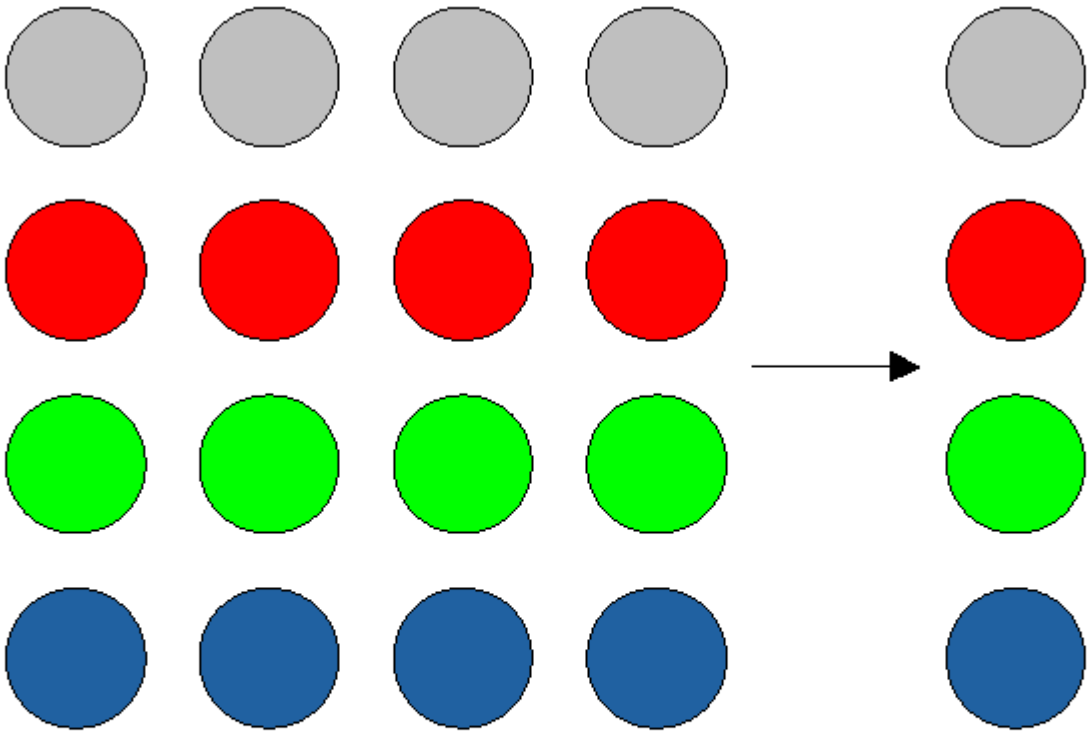


Fig. 12.11 Modified dependence graph with local interconnections.

Projection



Dependence graph Signal flow graph

Fig. 12.12 Projection of a dependence graph to a signal flow graph.

Direction Vectors

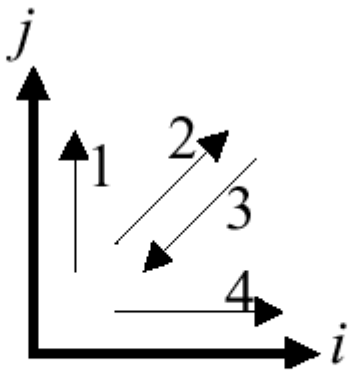


Fig. 12.13 Example vectors for direction representations.

Projection Vector

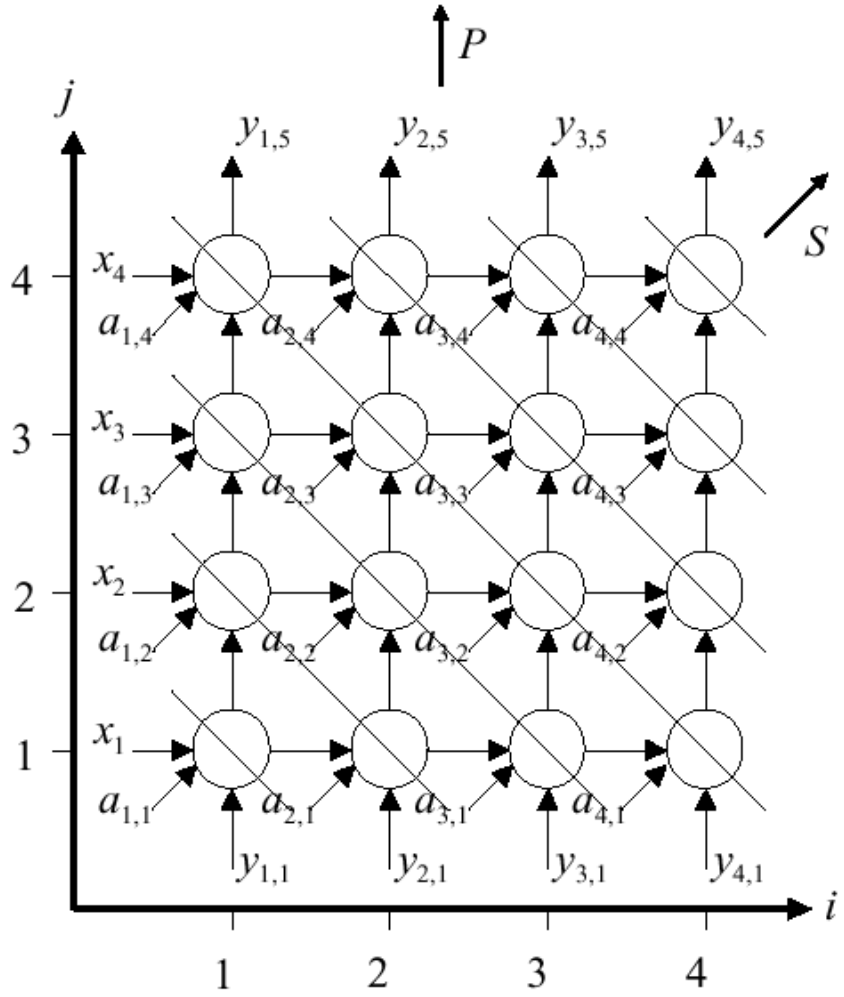


Fig. 12.14 Valid projection vector and hyperplane set.

Projections

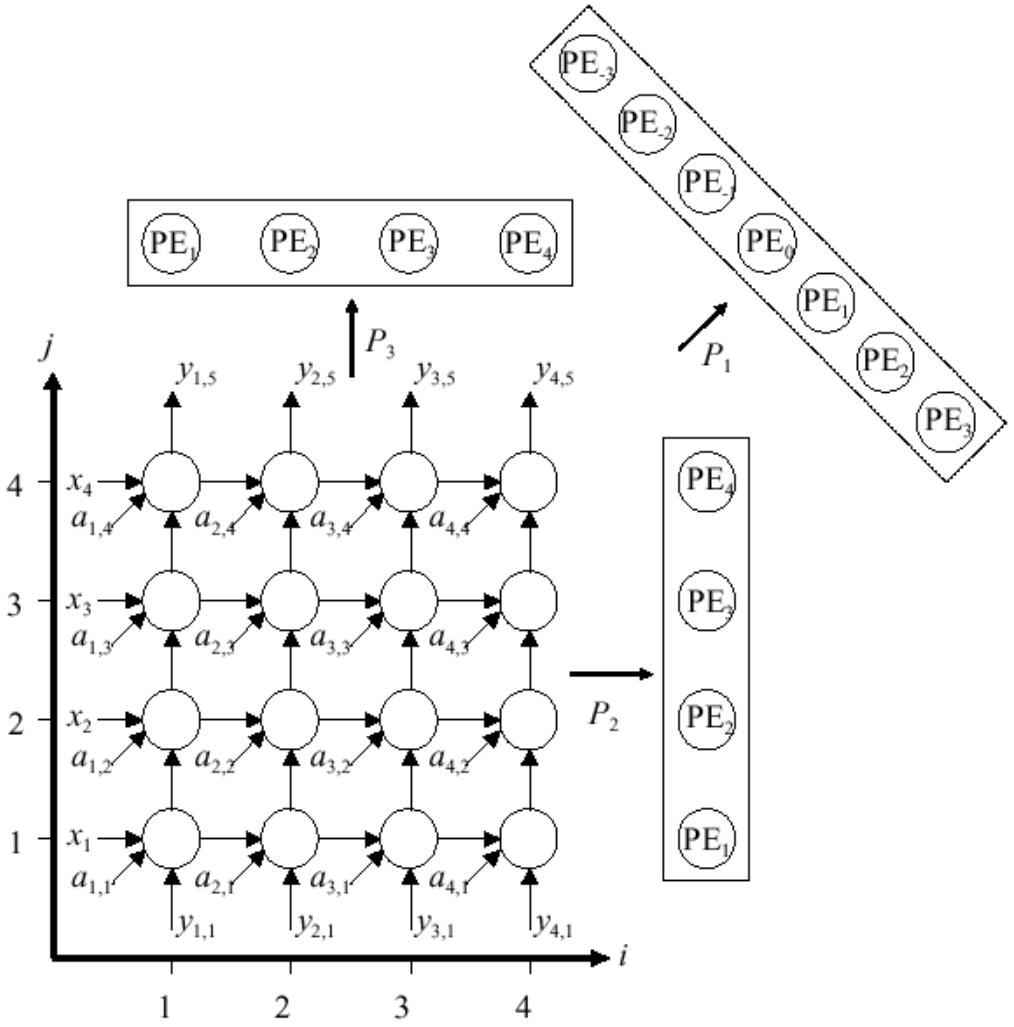


Fig. 12.15 Three different projections of a dependence graph.

Interconnection Mapping

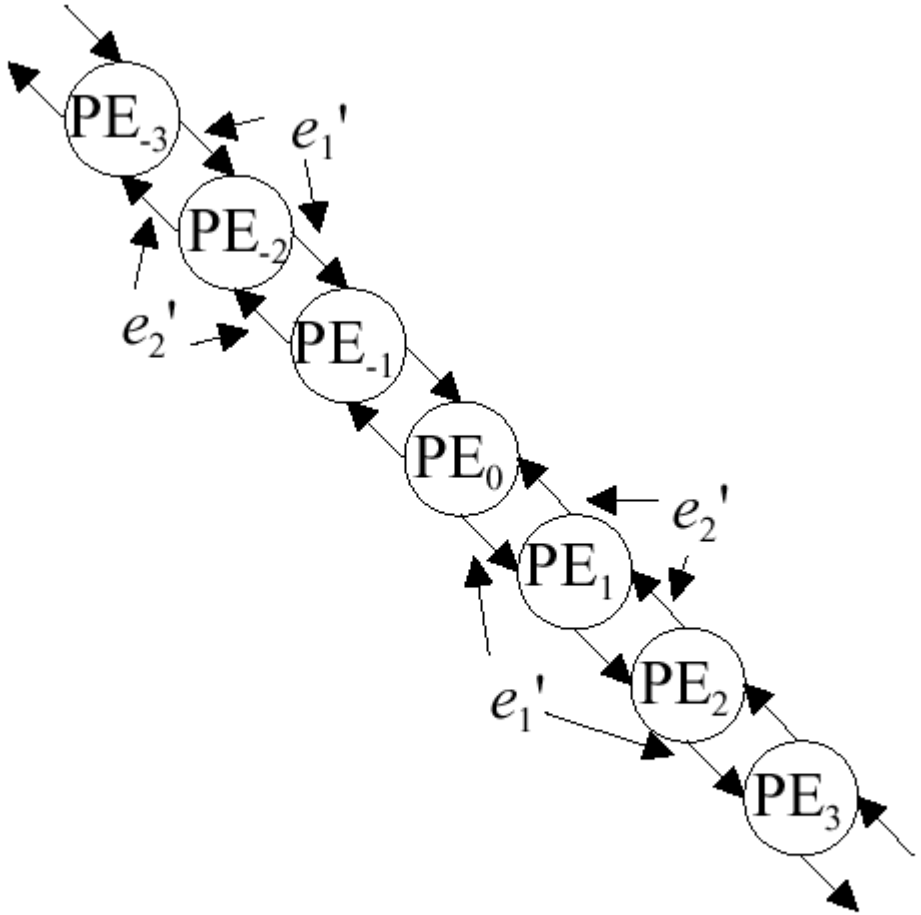


Fig. 12.16 Mapping of interconnections.

Interconnection Mapping

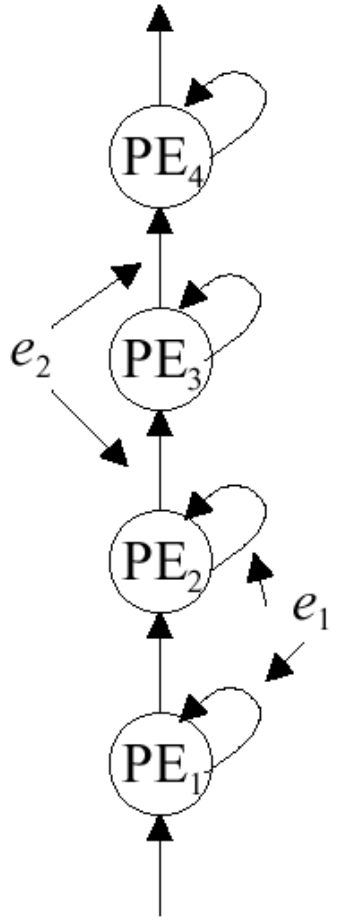


Fig. 12.17 Another interconnection mapping.

Array Processor I/O

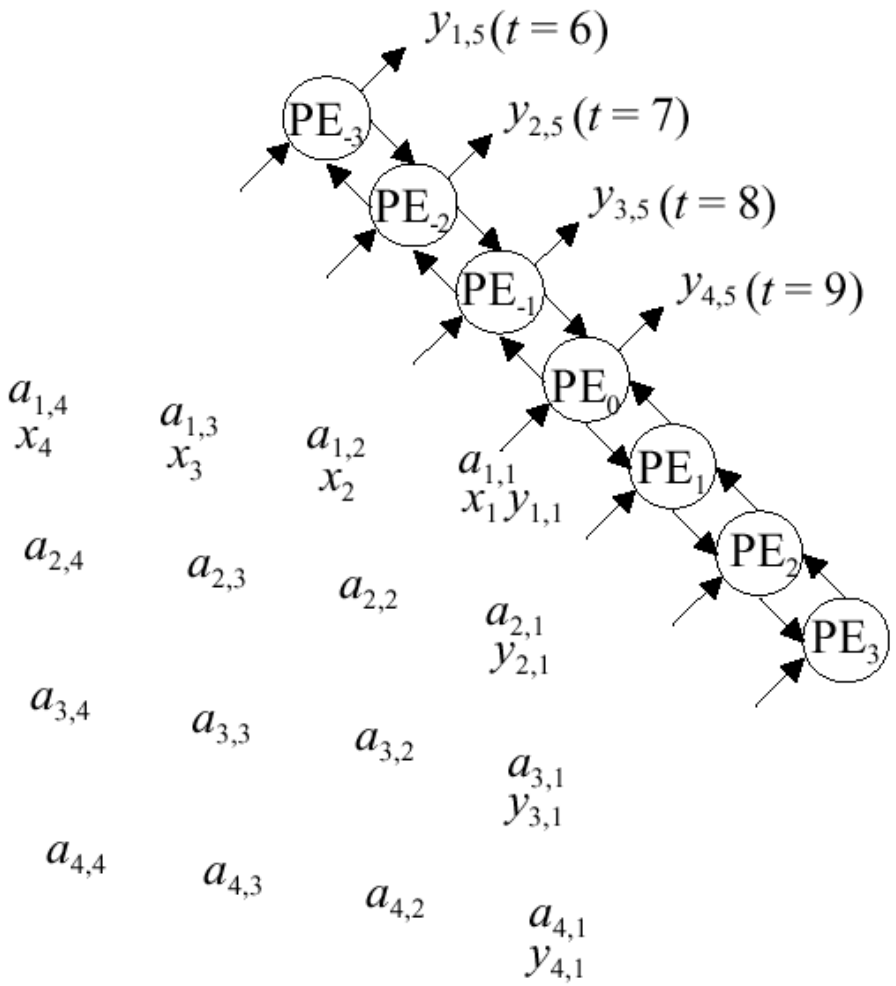


Fig. 12.18 I/O of the array processor.

Wavefront Array PE

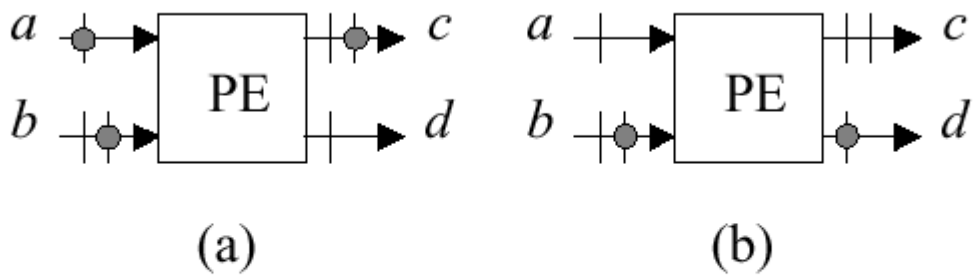


Fig. 12.19 PE used in a wavefront array: (a) a PE in activated state; and (b) a PE in waiting state.

Wavefront Array PE

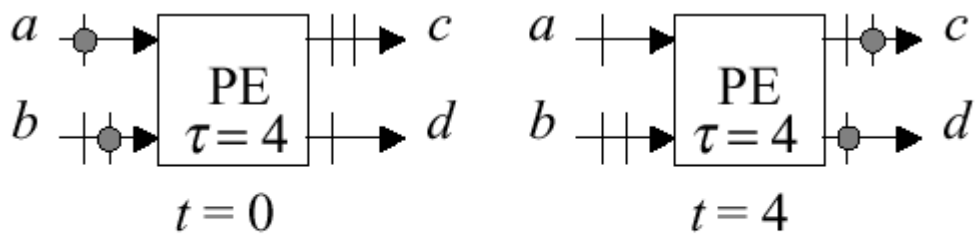


Fig. 12.20 Operations of a wavefront array PE.

Wavefront Array Processor

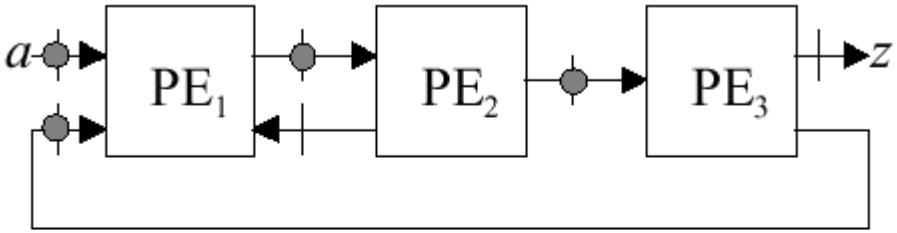


Fig. 12.21 Deadlock wavefront array processor.

Wavefront Array Processor

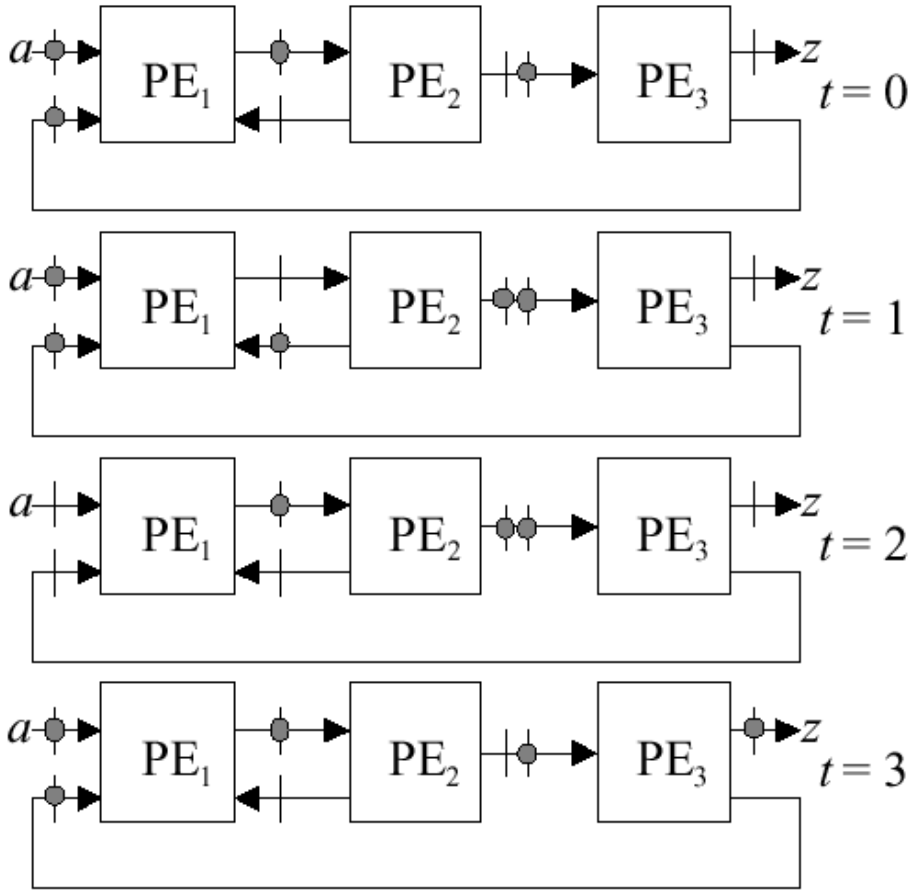


Fig. 12.22 Deadlock free wavefront array processor.

Wavefront Array Processor

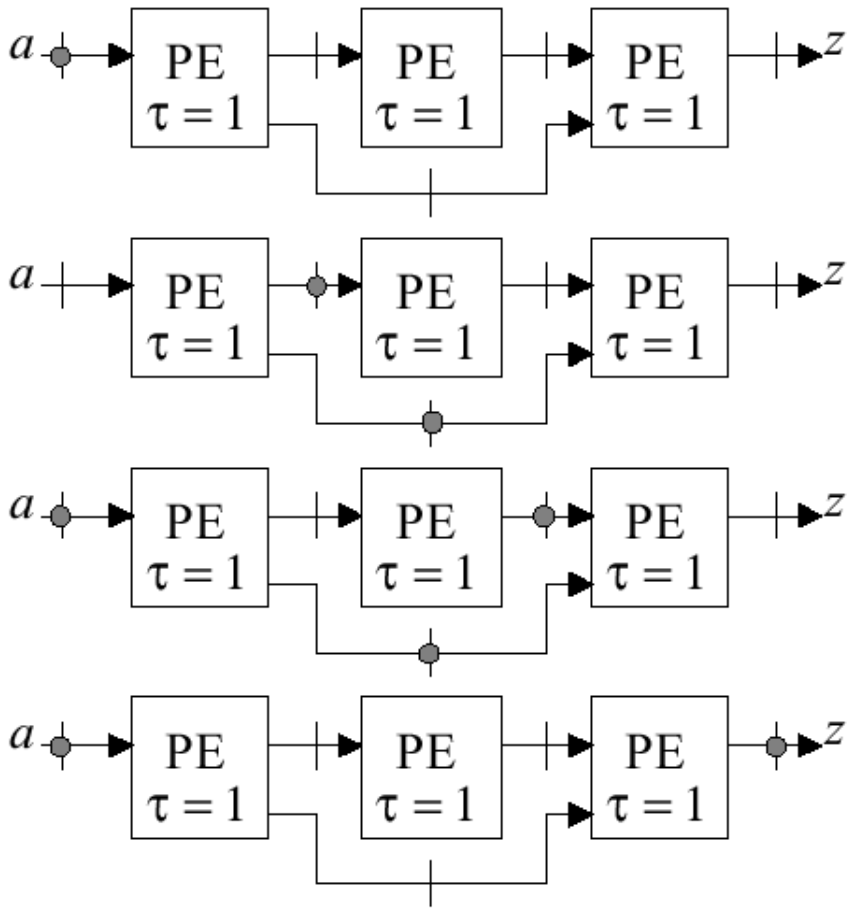


Fig. 12.23 Array processor with a throughput of 1/3.

Wavefront Array Processor

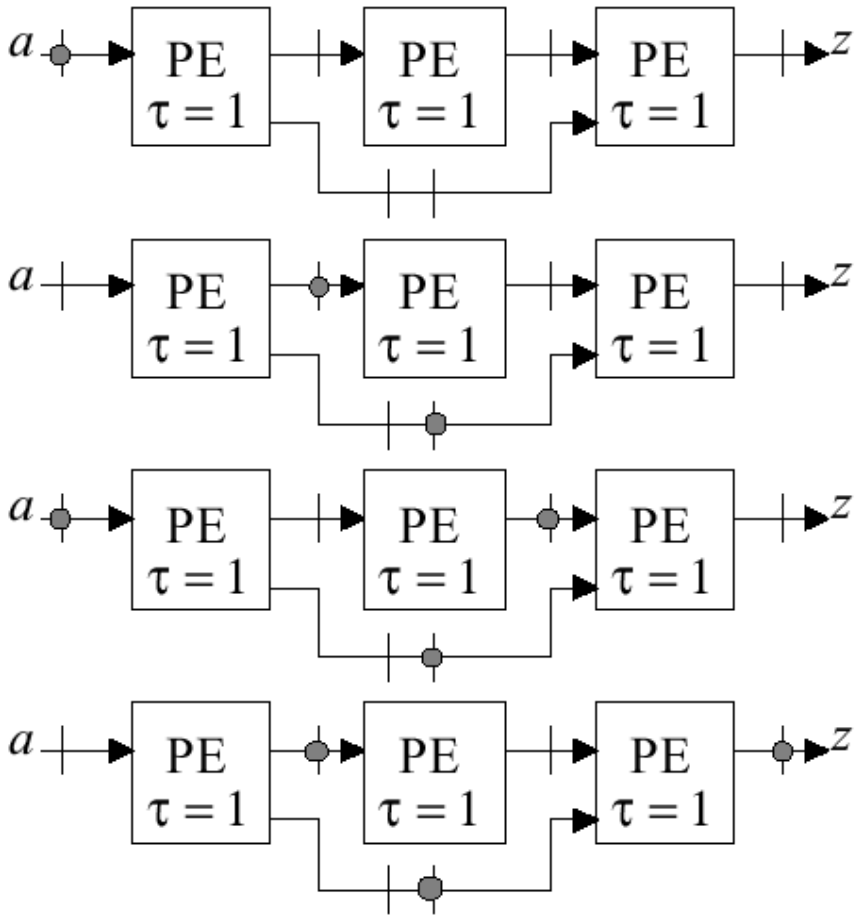


Fig. 12.24 Modified array processor with a throughput of 1/2.

Wavefront Array Processor

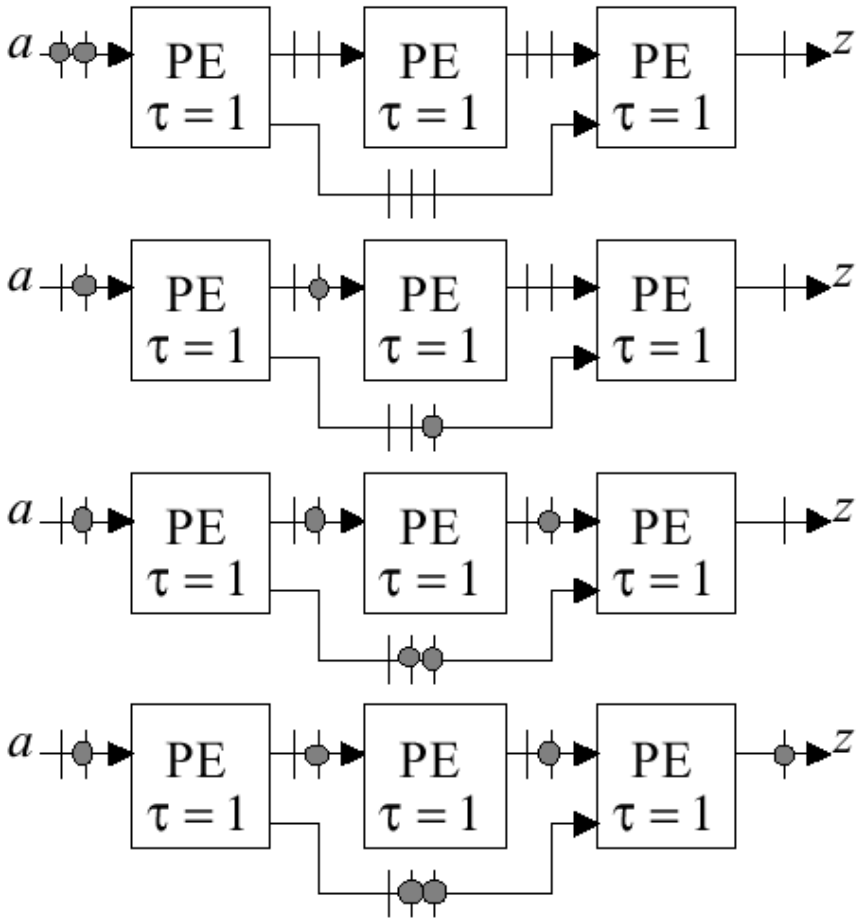


Fig. 12.25 Array processor with a throughput of 1.

Directed Cycle

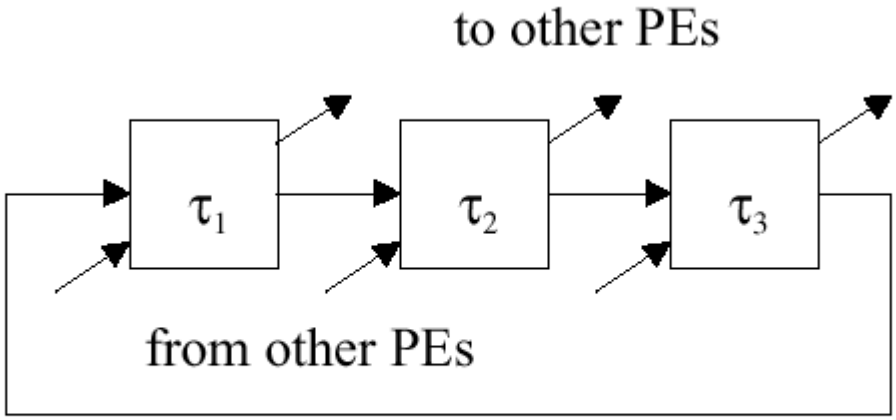


Fig. 12.26 Directed cycle in a wavefront array processor.

Undirected Cycle

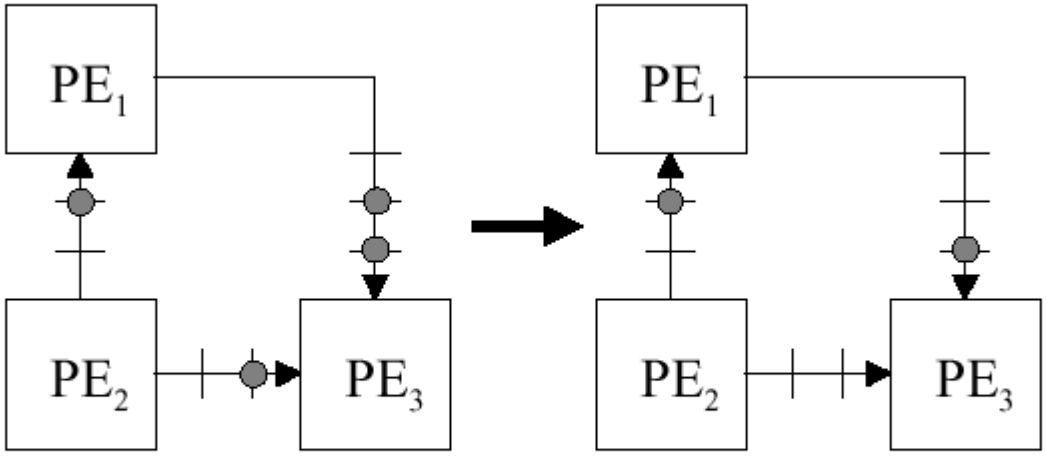


Fig. 12.27 An example demonstrating the undirected cycle property.

Pipelining Period Analysis

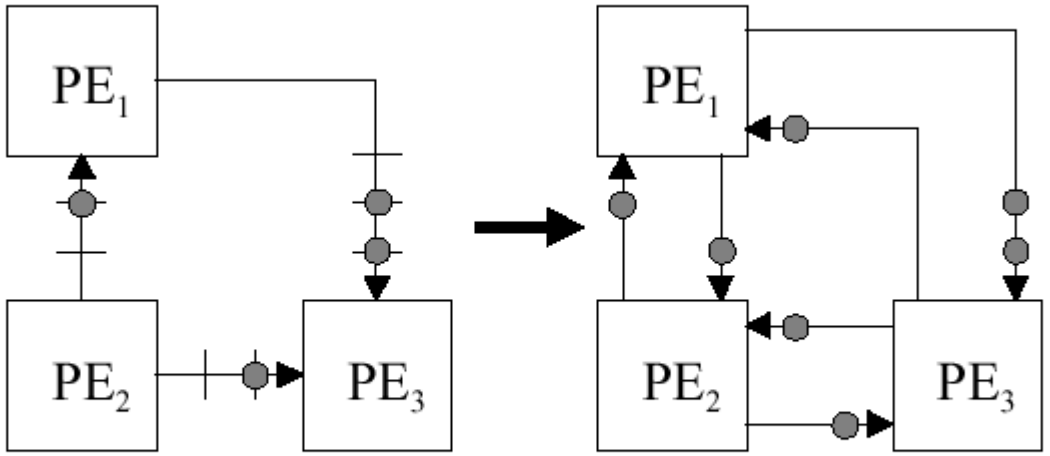


Fig. 12.28 Converting an array processor for pipelining period analysis.