Chapter 2

CMOS Logic Circuits

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NMOS Transistor

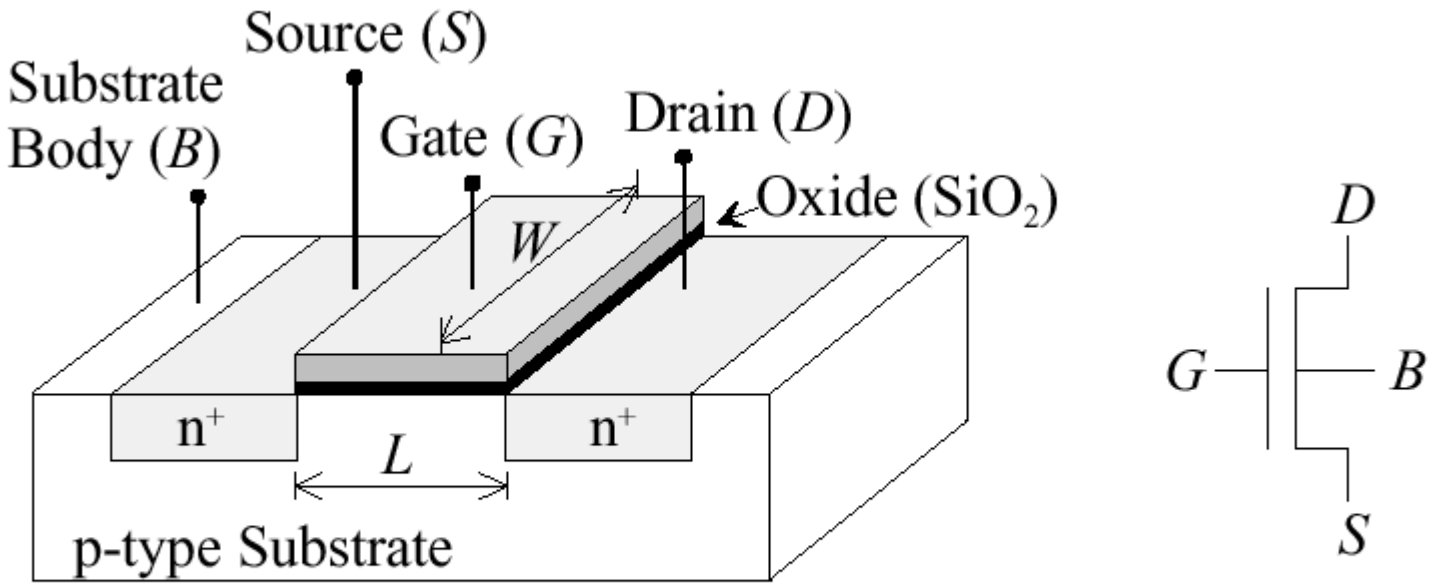

Fig. 2.1 Physical structure and circuit symbol of an nMOS transistor.

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NMOS Symbol

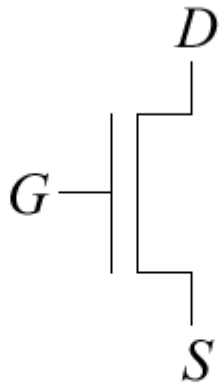

Fig. 2.2 Simplified nMOS transistor symbol.

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NMOS Model

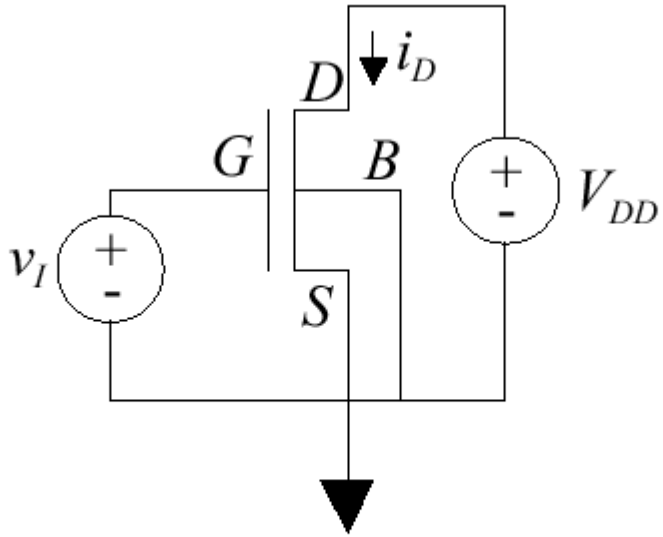

Fig. 2.3 Circuit for deriving the nMOS switch model.

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NMOS Switch

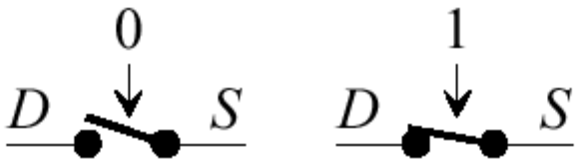

Fig. 2.4 Two operating modes of the digitally controlled nMOS switch model.

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PMOS Transistor

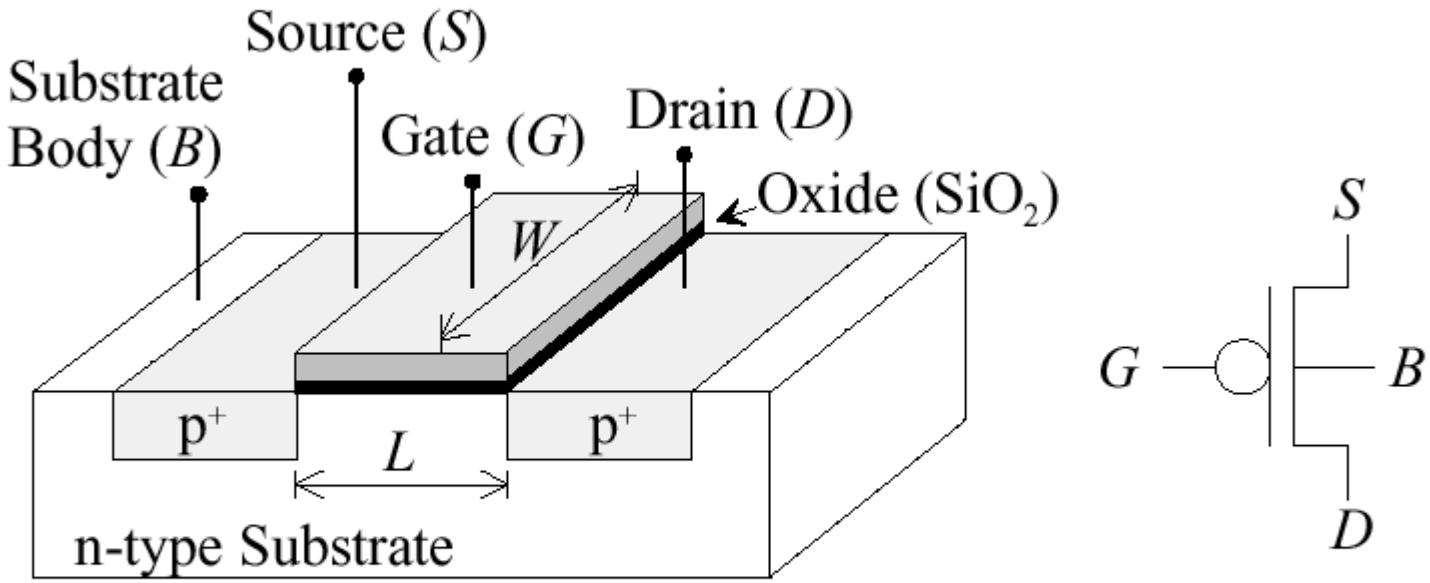

Fig. 2.5 Physical structure and circuit symbol of a pMOS transistor.

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PMOS Symbol

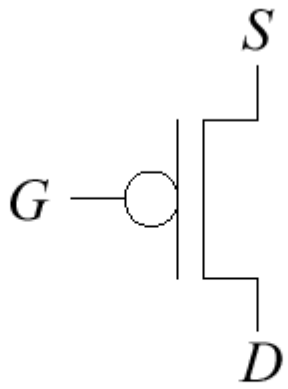

Fig. 2.6 Simplified pMOS transistor symbol.

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PMOS Model

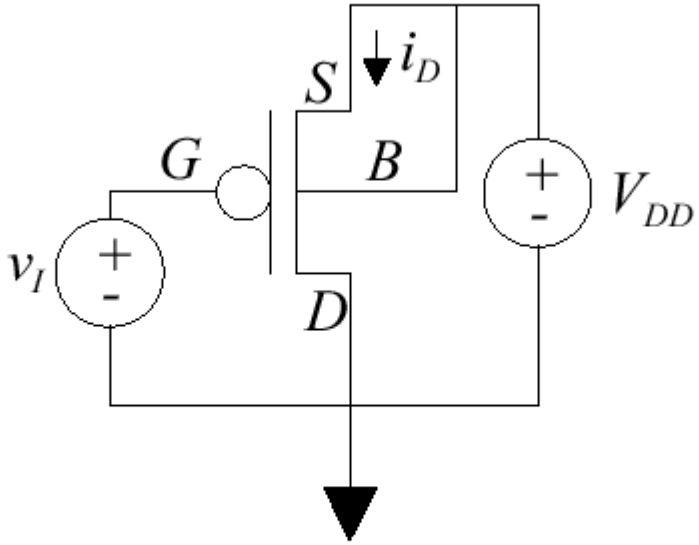

Fig. 2.7 Circuit for deriving the pMOS switch model.

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PMOS Switch

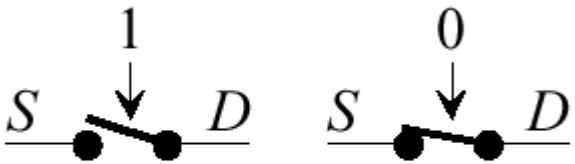

Fig. 2.8 Two operating modes of the digitally controlled pMOS switch model.

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MOSFET Switches

v_I	Logic Level	nMOS	pMOS
V_{DD}	1	ON	OFF
V_{SS}	0	OFF	ON

Fig. 2.9 Switch model of MOSFETs

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NMOS and PMOS

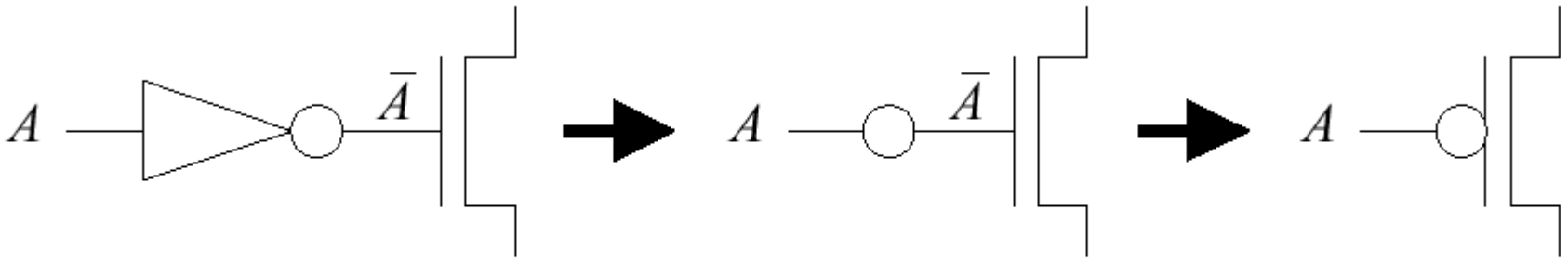

Fig. 2.10 Complementary relationship between nMOS and pMOS transistors.

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Inverter

A	*Z*
0	1
1	0

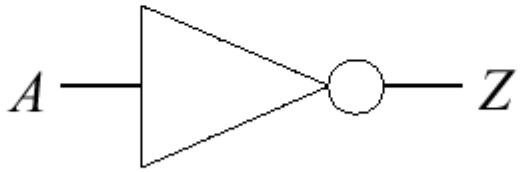

Fig. 2.11 Truth table and logic symbol of an inverter.

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Inverter Pull-Up

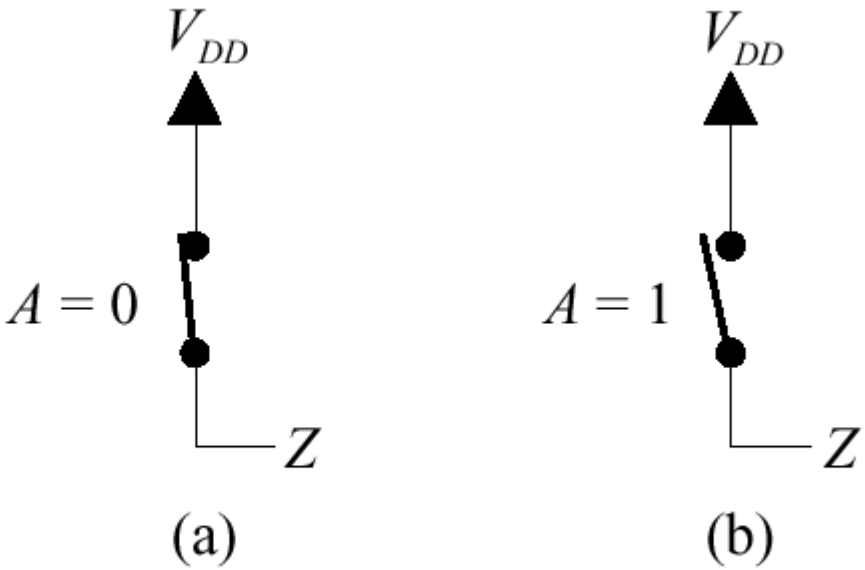

Fig. 2.12 Pull-up path of an inverter: (a) $A = 0$; (b) $A = 1$.

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Inverter Pull-Down

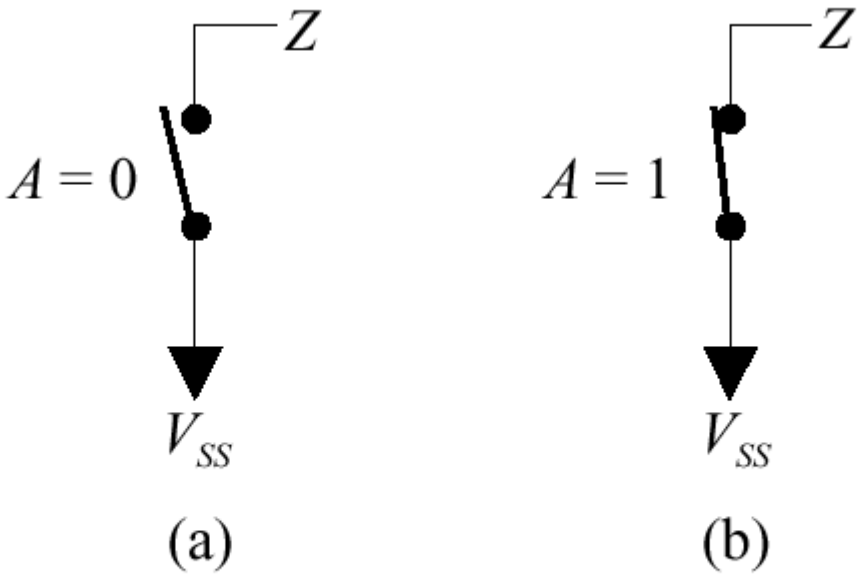

Fig. 2.13 Pull-down path of an inverter: (a) $A = 0$; (b) $A = 1$.

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Inverter

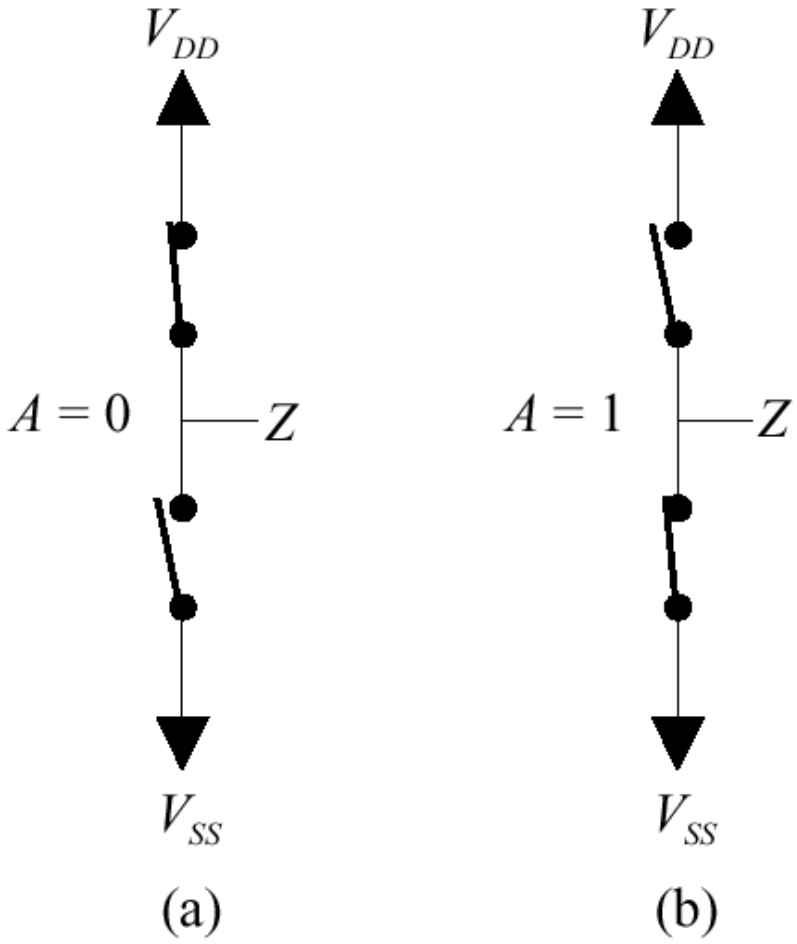

Fig. 2.14 Switch network implementing an inverter: (a) $A = 0$; (b) $A = 1$.

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Inverter

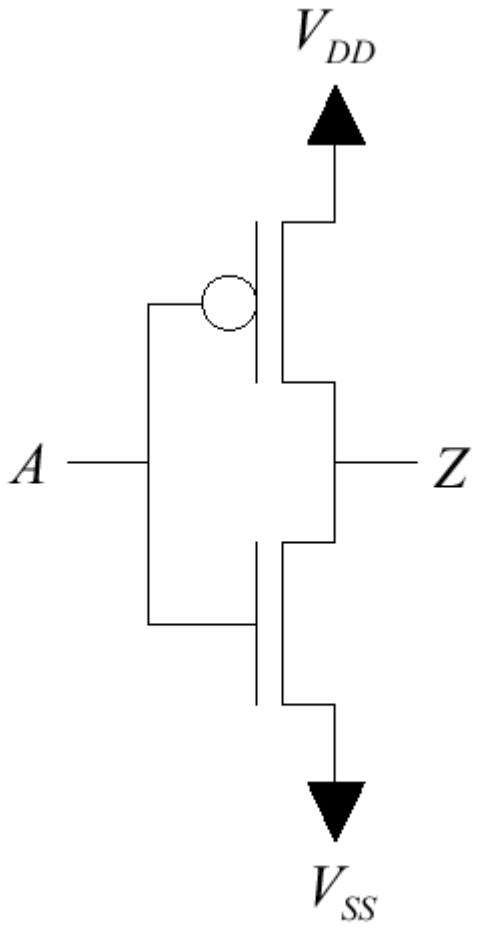

Fig. 2.15 CMOS inverter.

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CMOS Logic Structures

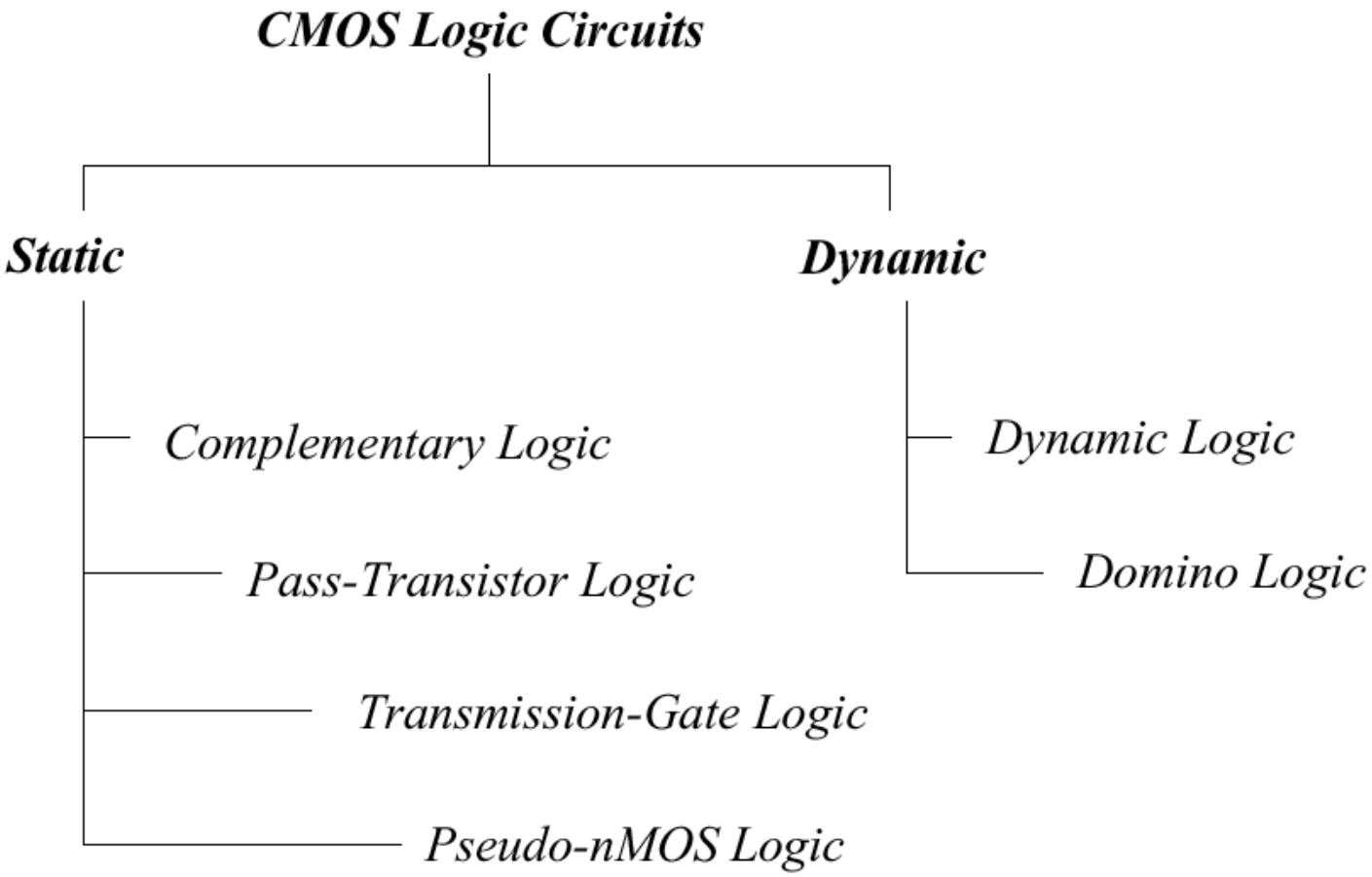

Fig. 2.16 Different structures of CMOS logic circuits.

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Complementary Logic

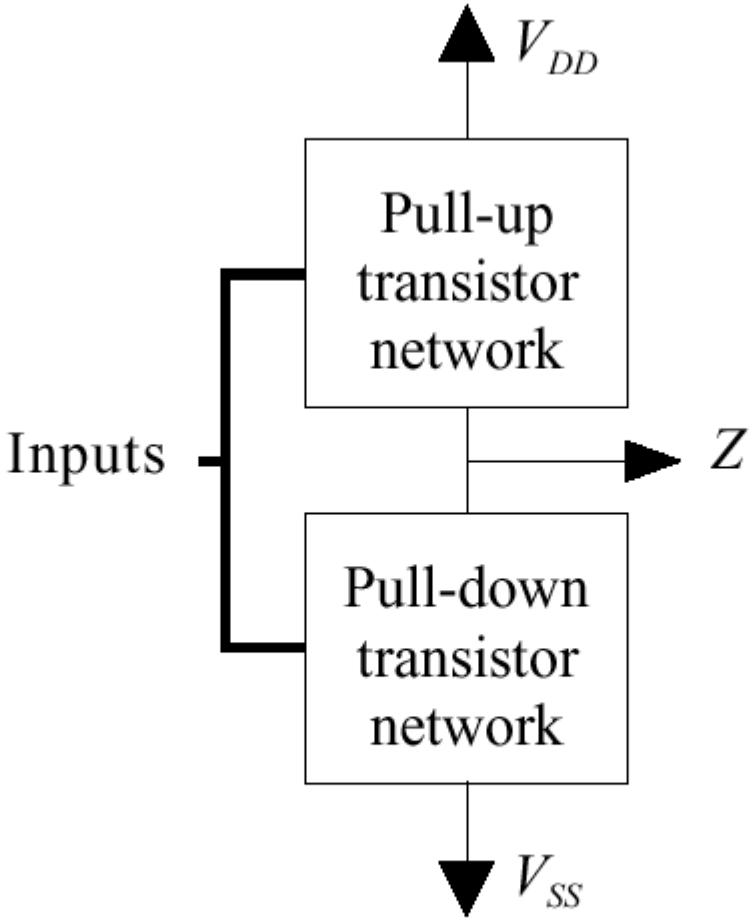

Fig. 2.17 General structure of CMOS complementary logic circuit.

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Serial Network

Fig. 2.18 Serial switch network.

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Parallel Network

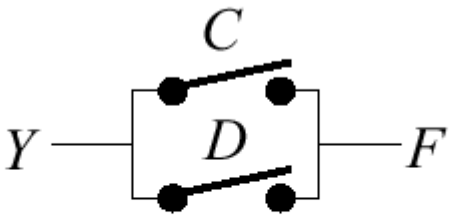

Fig. 2.19 Parallel switch network.

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NMOS Output

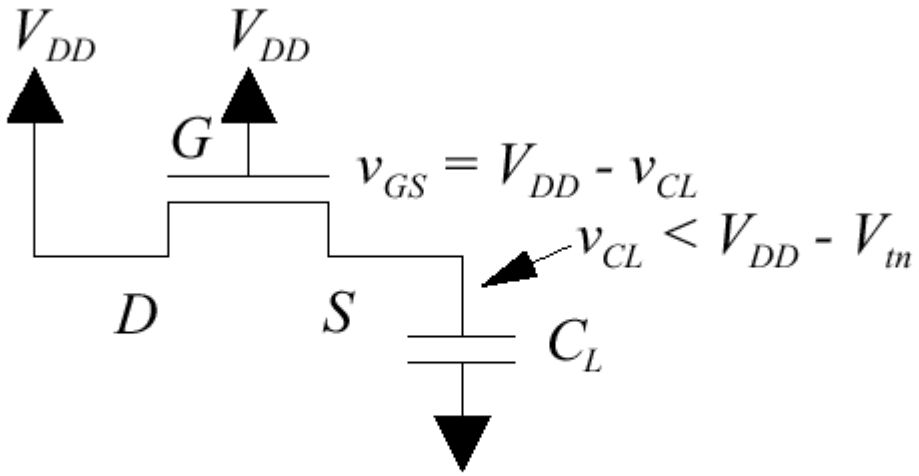

Fig. 2.20 Output connected to V_{DD} through an nMOS transistor.

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PMOS Output

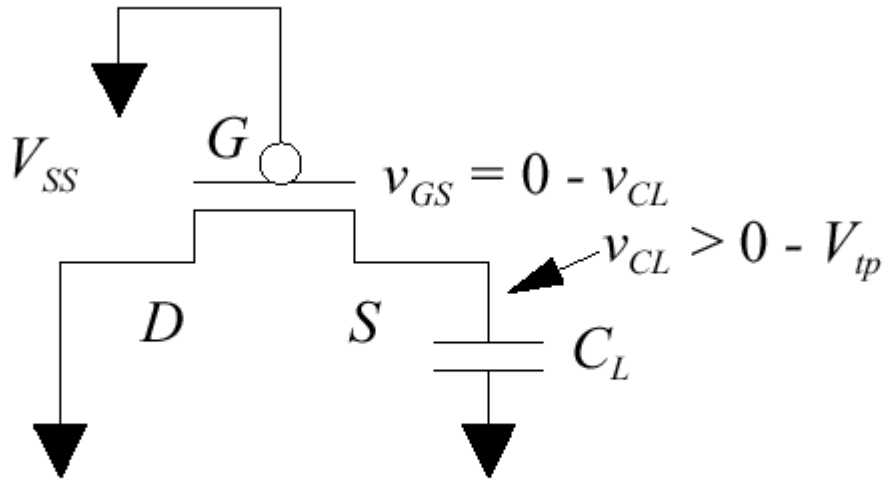

Fig. 2.21 Output connected to V_{SS} through a pMOS transistor.

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Logic Swing

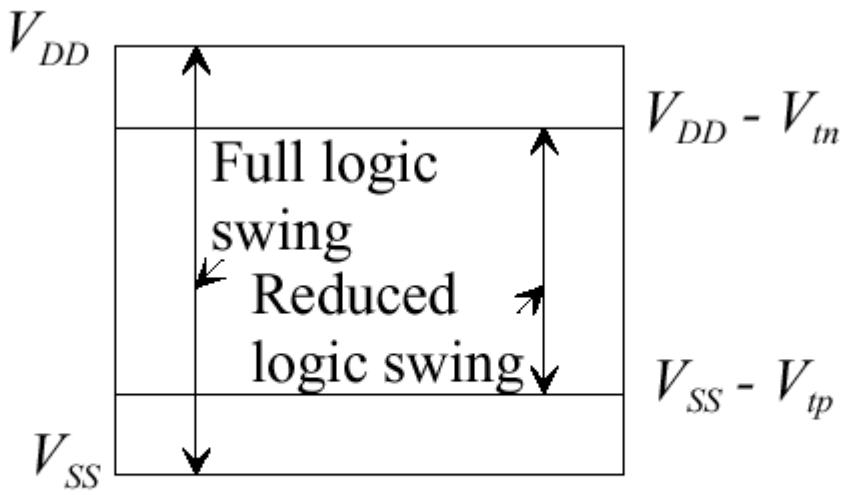

Fig. 2.22 Full logic swing and reduced logic swing.

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NAND Pull-Up Network

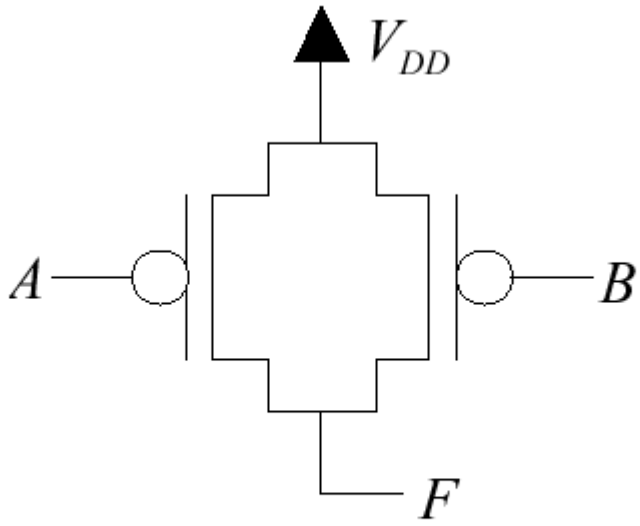

Fig. 2.24 Pull-up network for $F = \overline{AB}$.

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NAND Pull-Down Network

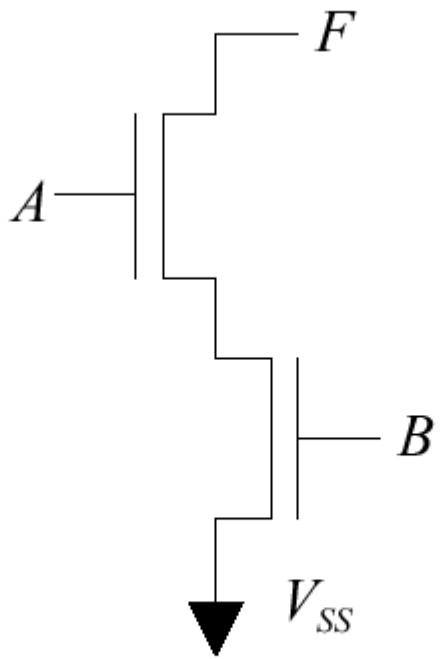

Fig. 2.25 Pull-down network for $F = \overline{AB}$.

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NAND Gate

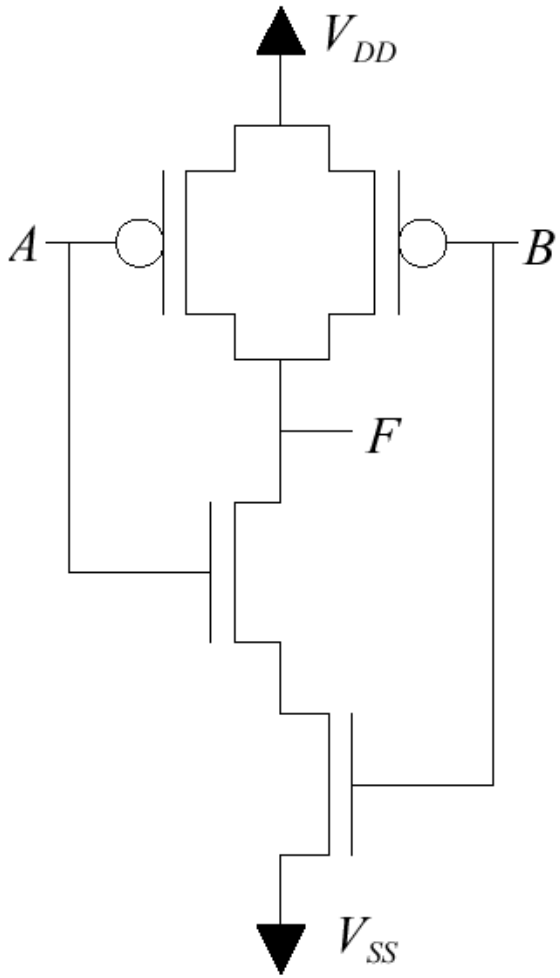

Fig. 2.26 Transistor schematic diagram of a two-input NAND gate.

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Pull-Up and Pull-Down Networks

Pull-up network	Pull-down network
pMOS transistor	nMOS transistor
serial connection	parallel connection
parallel connection	serial connection

Fig. 2.27 Complementary pull-up and pull-down networks in a logic circuit.

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NOR Gate

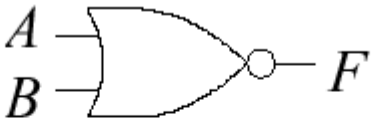

Fig. 2.28 Logic symbol of a two-input NOR gate.

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NOR Pull-Up Network

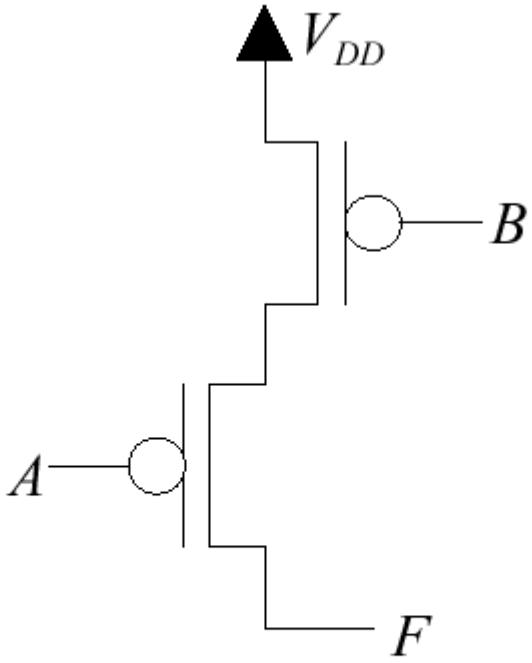

Fig. 2.29 Pull-up network for $F = \overline{A + B}$.

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NOR Gate

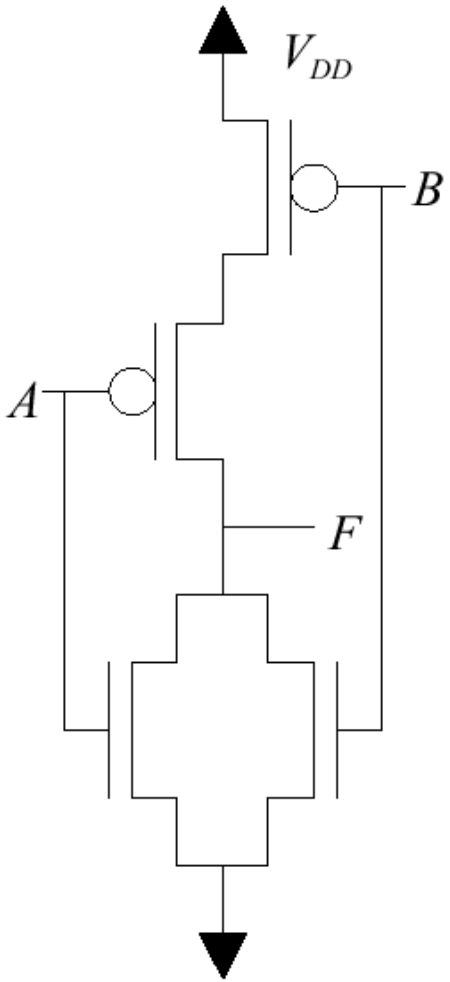

Fig. 2.30 CMOS two-input NOR gate.

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Example 2.3

A	B	C	D	F
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

Fig. 2.31 Truth table of F in Example 2.3.

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Example 2.3

F	AB = 00	AB = 01	AB = 11	AB = 10
CD = 00	1	1	0	1
CD = 01	1	1	0	1
CD = 11	1	1	0	0
CD = 10	1	1	0	1

Fig. 2.32 Karnaugh map of F in Example 2.3.

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Example 2.3

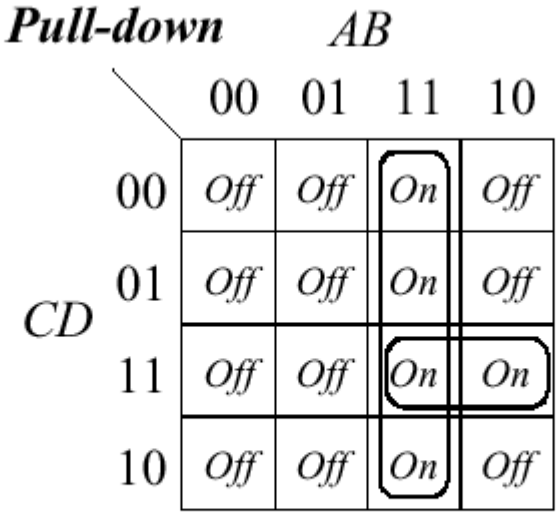

Fig. 2.33 Karnaugh map for the pull-down network in Example 2.3.

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Example 2.3

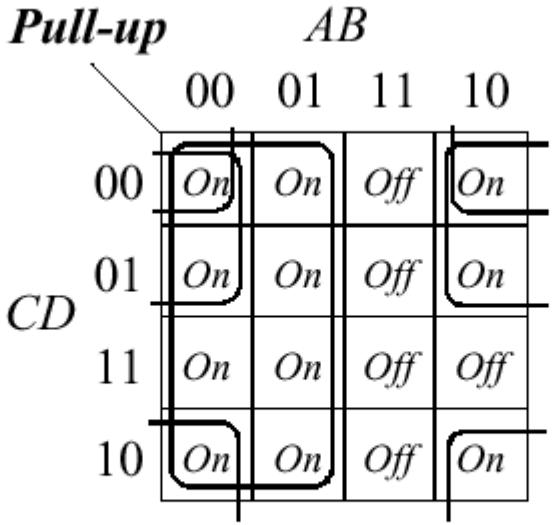

Fig. 2.34 Karnaugh map for the pull-up network in Example 2.3.

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Logic Circuit

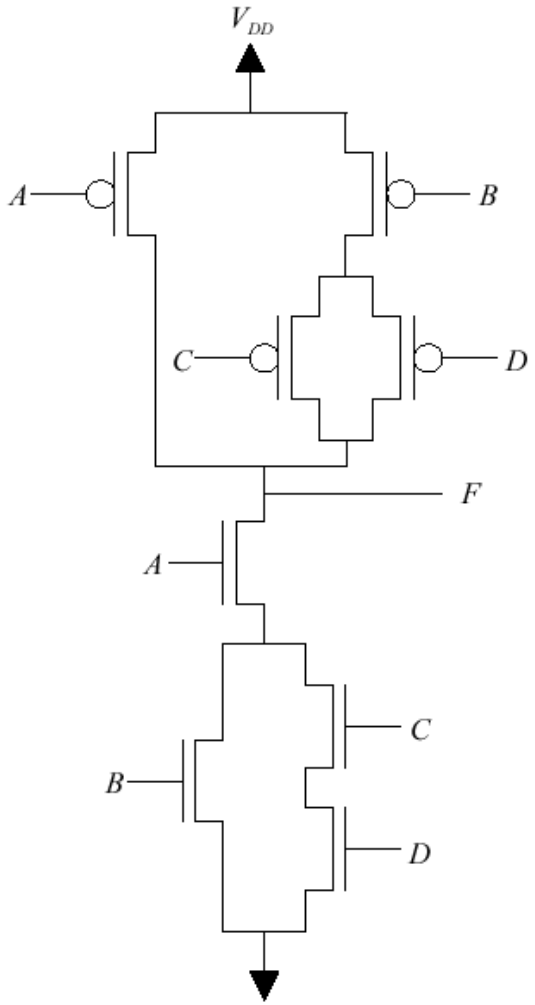

Fig. 2.35 Logic circuit for function $F = \overline{A(B+CD)}$.

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Example 2.4

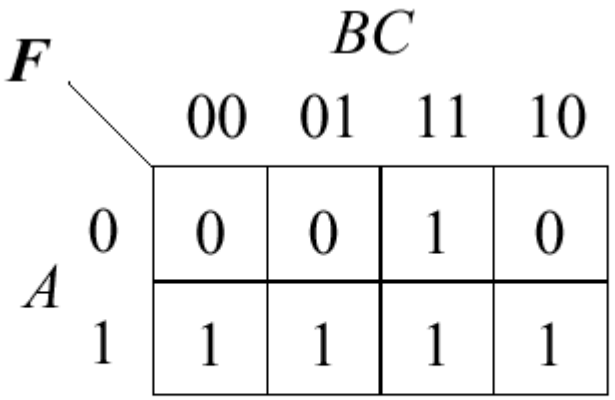

Fig. 2.36 Karnaugh map of F in Example 1.4.

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Example 2.4

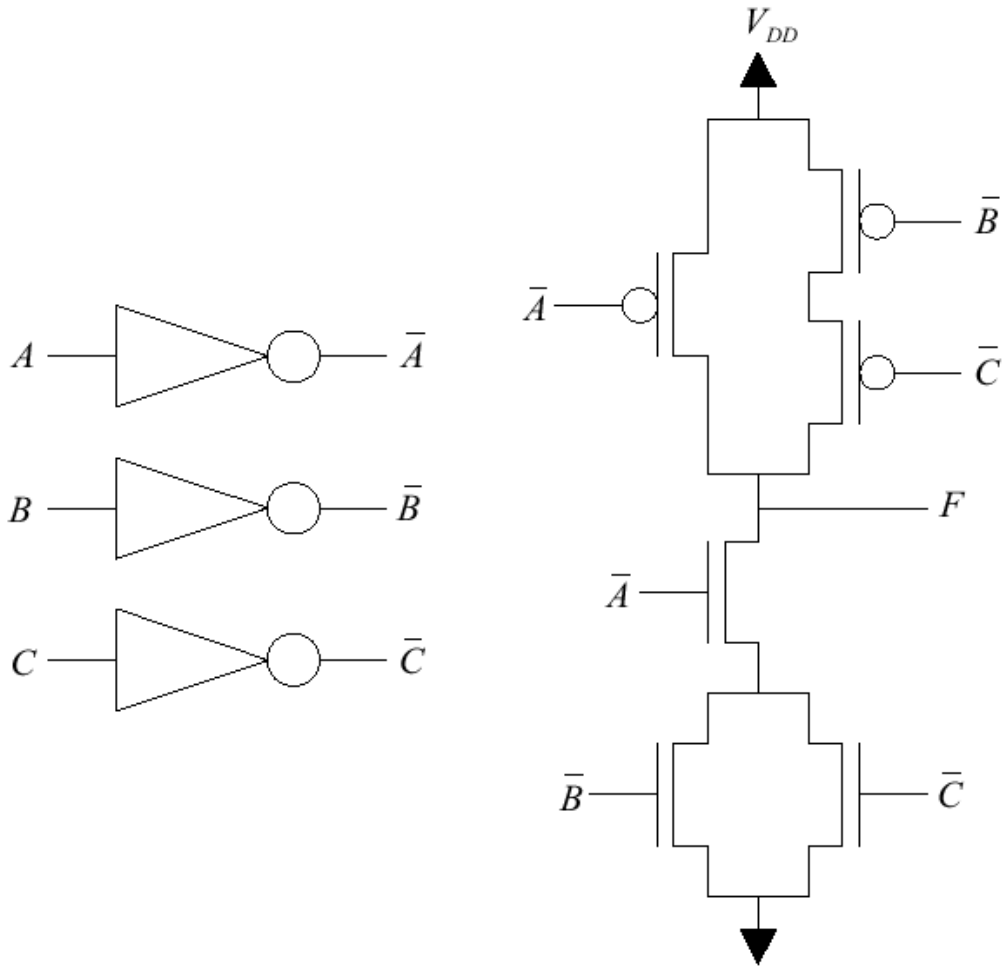

Fig. 2.37 Logic circuit designed for Example 2.4.

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Example 2.4

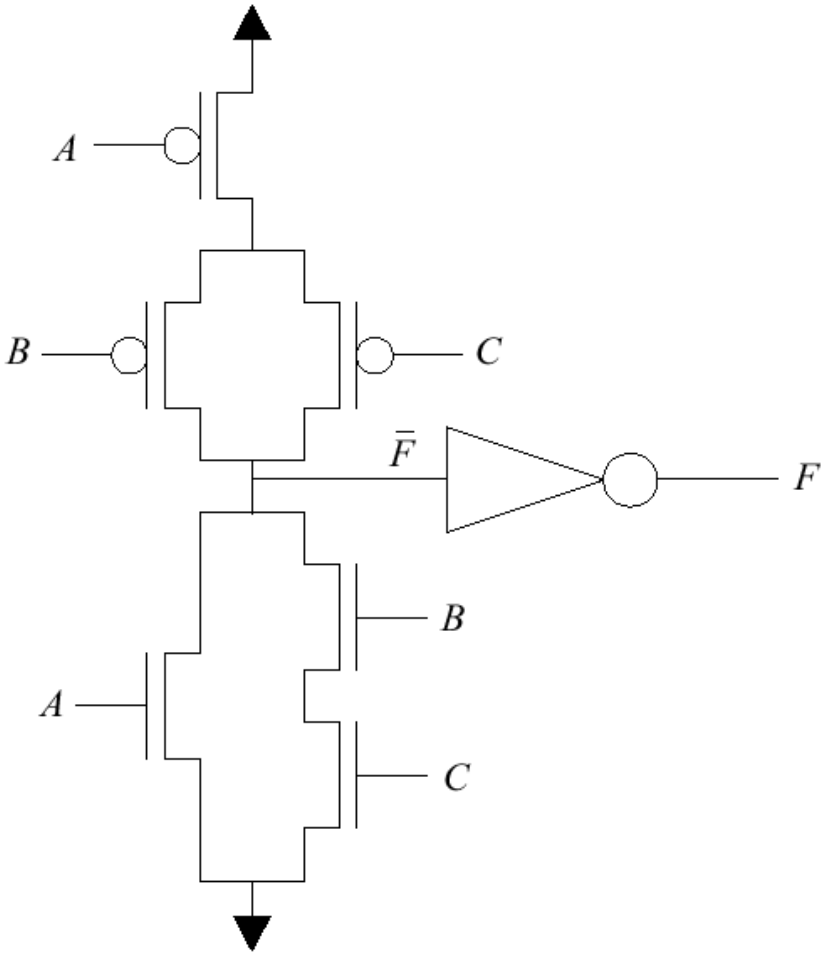

Fig. 2.38 Minimized logic circuit for Example 2.4.

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2-to-1 Multiplexer

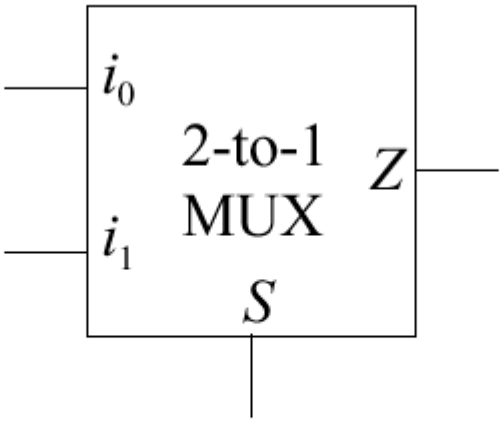

Fig. 2.39 Symbol of a 2-to-1 multiplexer (MUX).

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2-to-1 Multiplexer

S	i_0	i_1	Z
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

Fig. 2.40 Truth table of a 2-to-1 MUX.

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2-to-1 Multiplexer

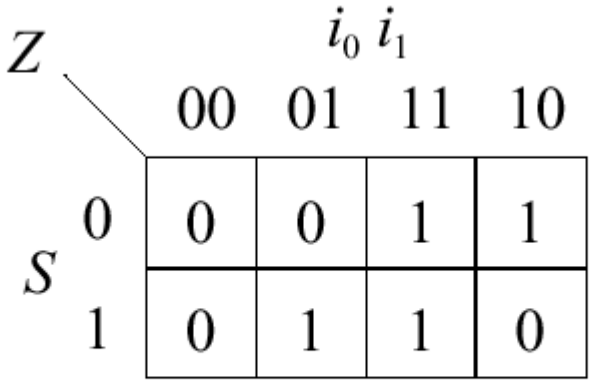

Fig. 2.41 Karnaugh map of a 2-to-1 MUX.

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2-to-1 Multiplexer

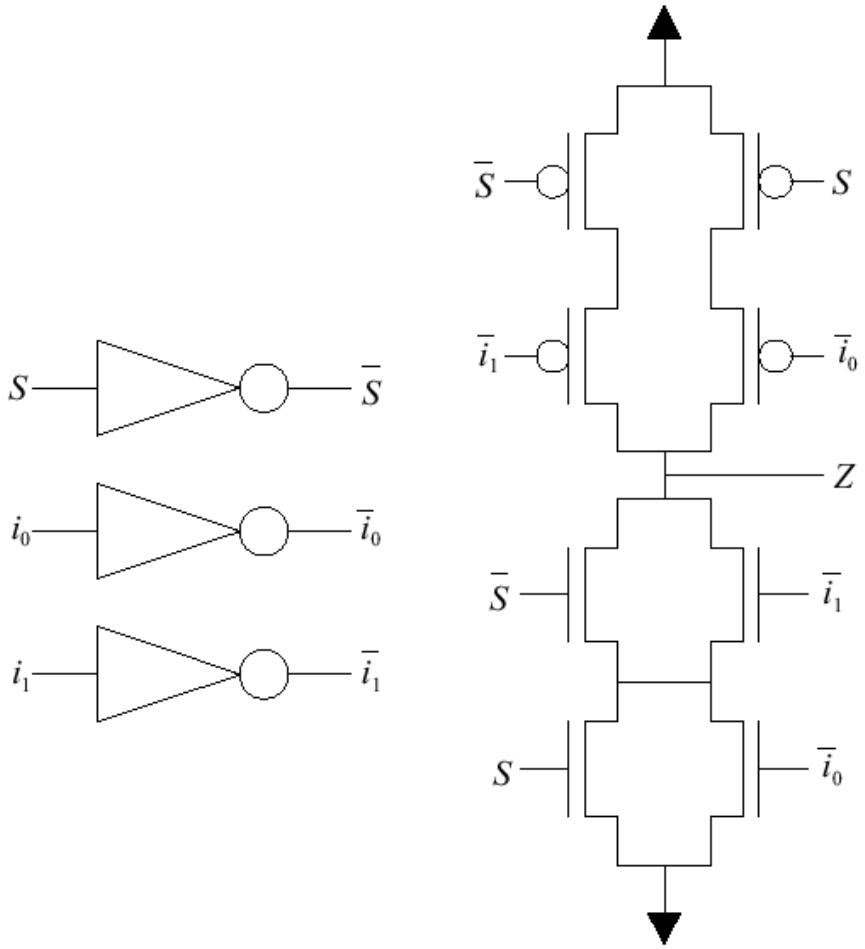

Fig. 2.42 Complementary logic circuit for a 2-to-1 multiplexer.

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2-to-1 Multiplexer

S	Z
0	i_0
1	i_1

Fig. 2.43 Modified truth table of a 2-to-1 multiplexer.

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2-to-1 Multiplexer

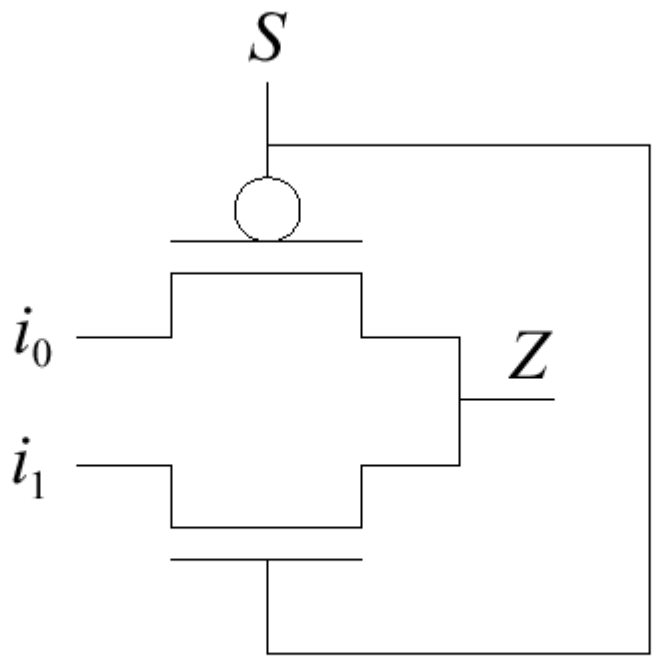

Fig. 2.44 Pass-transistor logic for a 2-to-1 multiplexer.

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Trickle Transistor

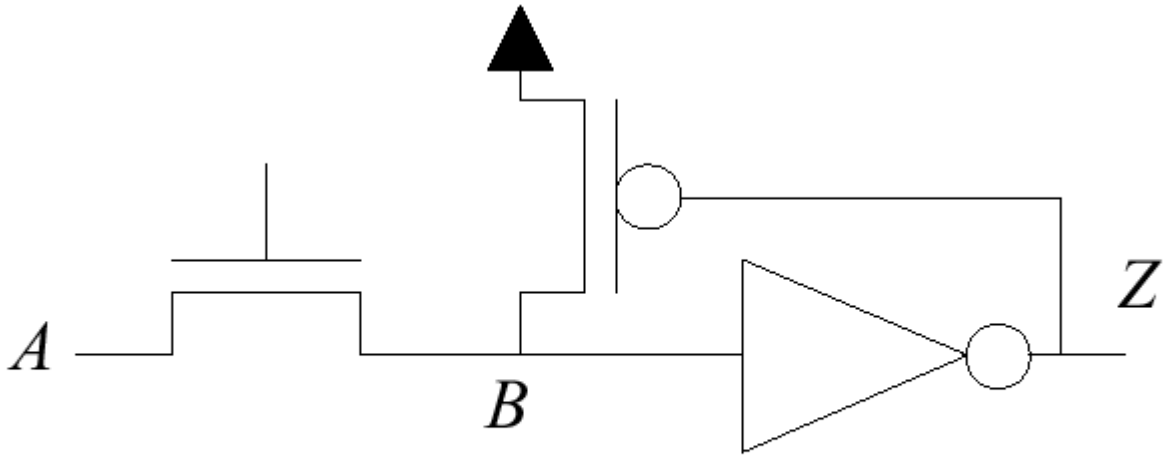

Fig. 2.45 Trickle transistor used to restore logic level.

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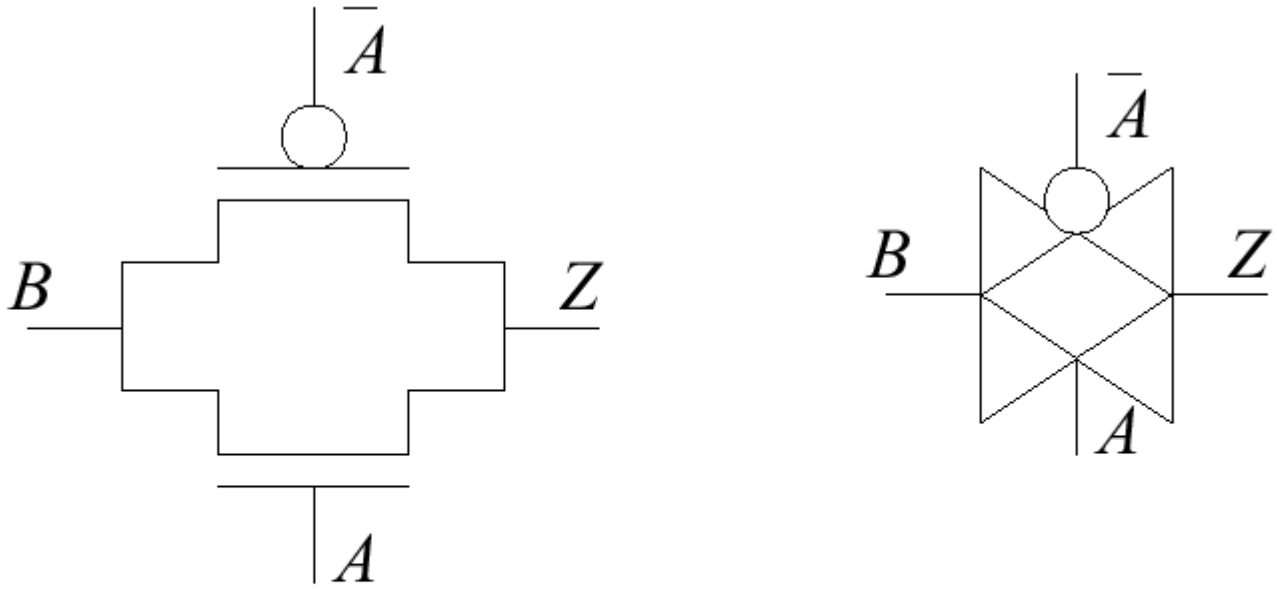
T-Gate



Schematic Symbol

Fig. 2.46 Transmission-gate (t-gate) structure and its symbol.

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2-to-1 Multiplexer

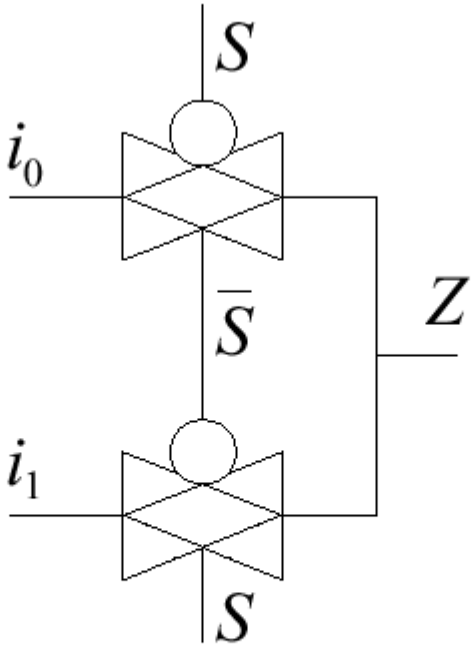

Fig. 2.47 Transmission-gate logic for a 2-to-1 multiplexer.

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4-to-1 Multiplexer

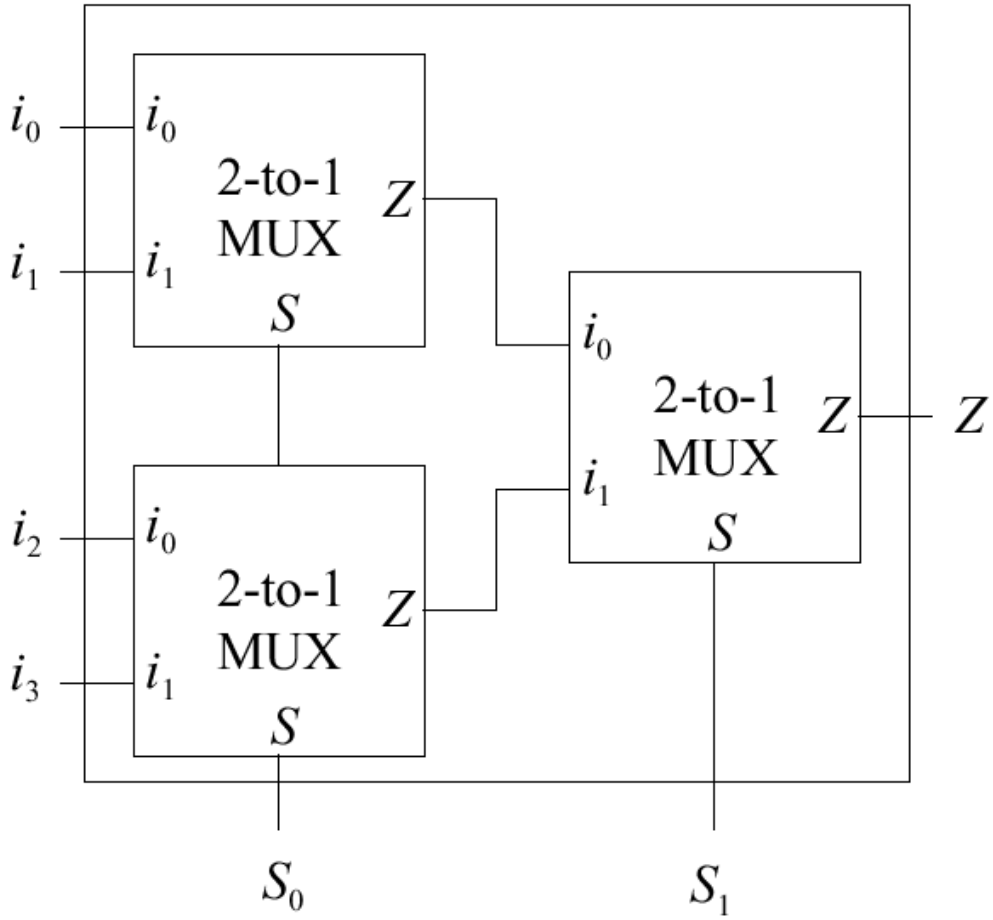

Fig. 2.48 4-to-1 multiplexer.

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8-to-1 Multiplexer

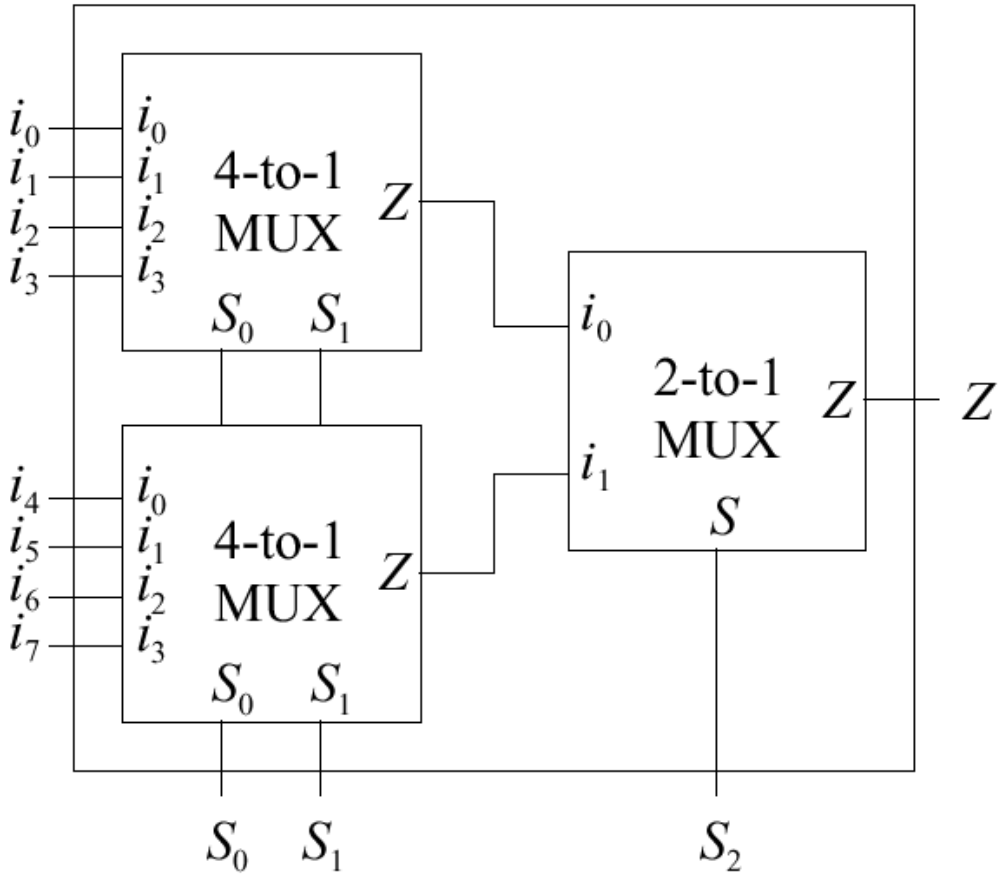

Fig. 2.49 8-to-1 multiplexer.

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Hard-Wired Multiplexer

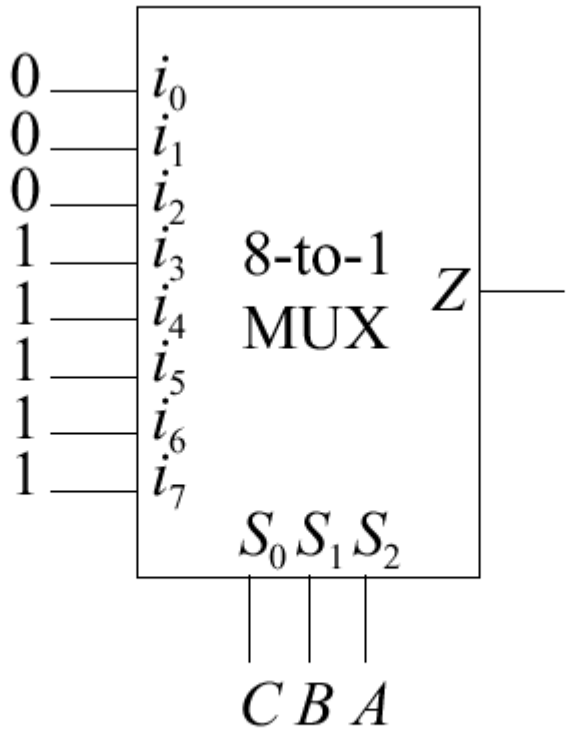

Fig. 2.50 Multiplexer hard-wired to implement $F = A + BC$.

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Configurable Logic Block

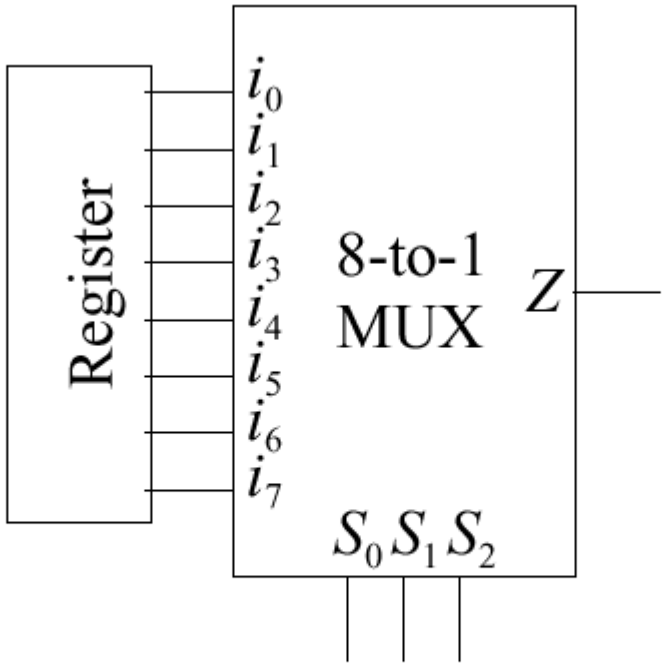

Fig. 2.51 A multiplexer-based configurable logic block.

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AND Gate

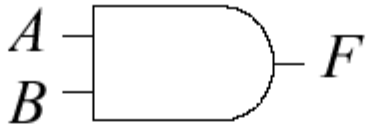

Fig. 2.52 Logic symbol of a two-input AND gate.

A	B	F
0	0	0
0	1	0
1	0	0
1	1	1

Fig. 2.53 Truth table of $F = AB$ in Example 1.5.

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AND Gate

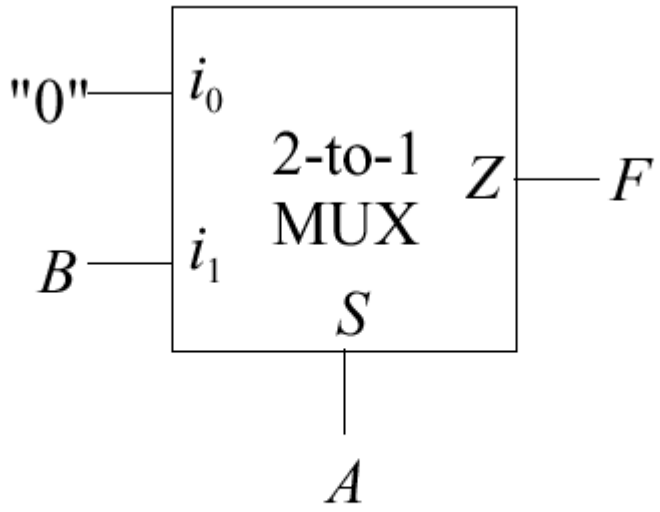

Fig. 2.54 2-to-1 multiplexer implementing a two-input AND gate.

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Example 2.6

A	B	C	F
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

Fig. 2.55 Truth table of $F = \overline{A}(B + \overline{C}) + A\overline{B}C$.

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Example 2.6

A	B	F
0	0	$\overline{C}$
0	1	1
1	0	C
1	1	0

Fig. 2.56 Modified truth table of $F = \overline{A}(B + \overline{C}) + A\overline{B}C$ in Example 1.6.

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Tri-State Inverter

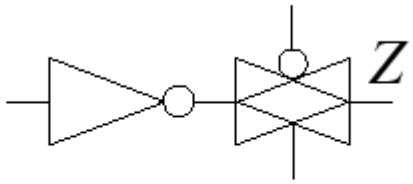

Fig. 2.58 Tri-state inverter.

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