Chapter 5

Sequential Logic Circuits

Clock Signal

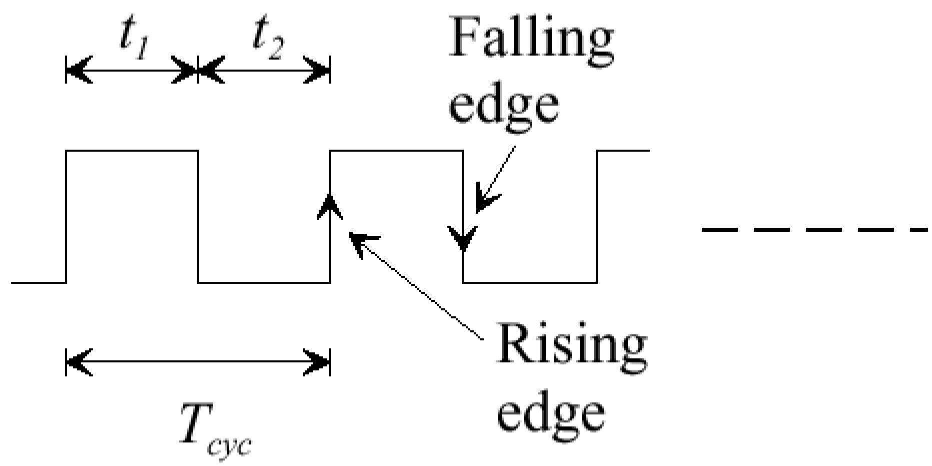


Fig. 5.1 Clock signal.

Rise/Fall Time

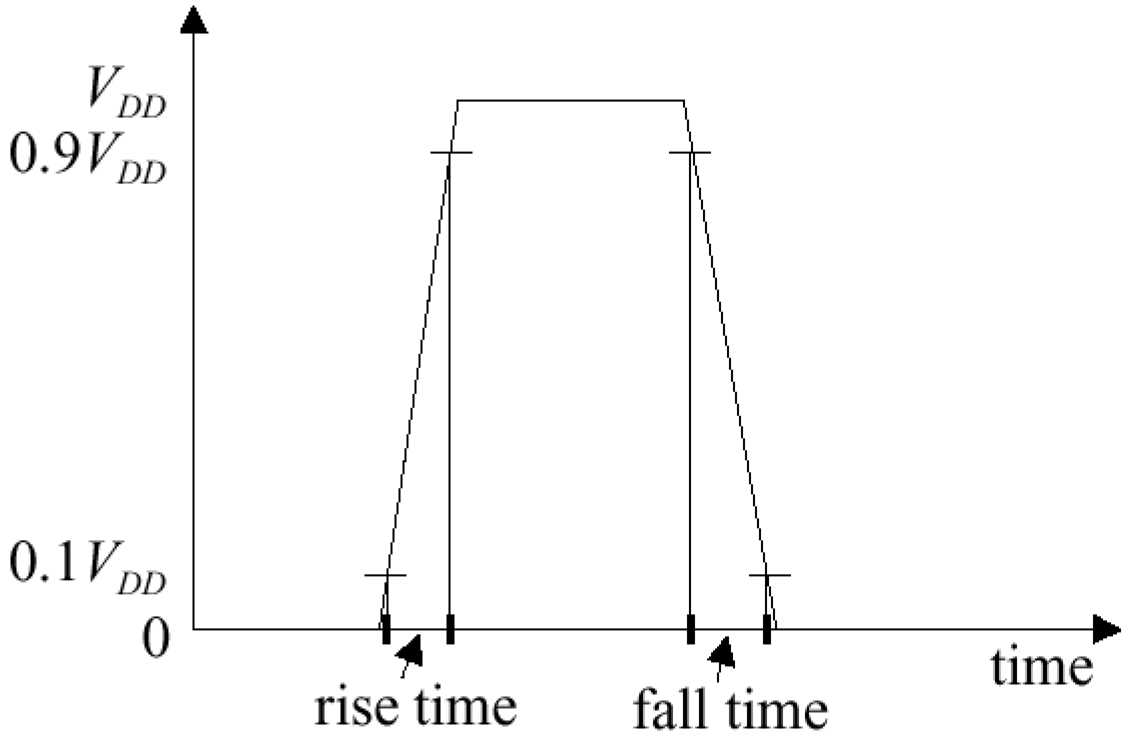


Fig. 5.2 Rise time and fall time.

Sequential Circuit

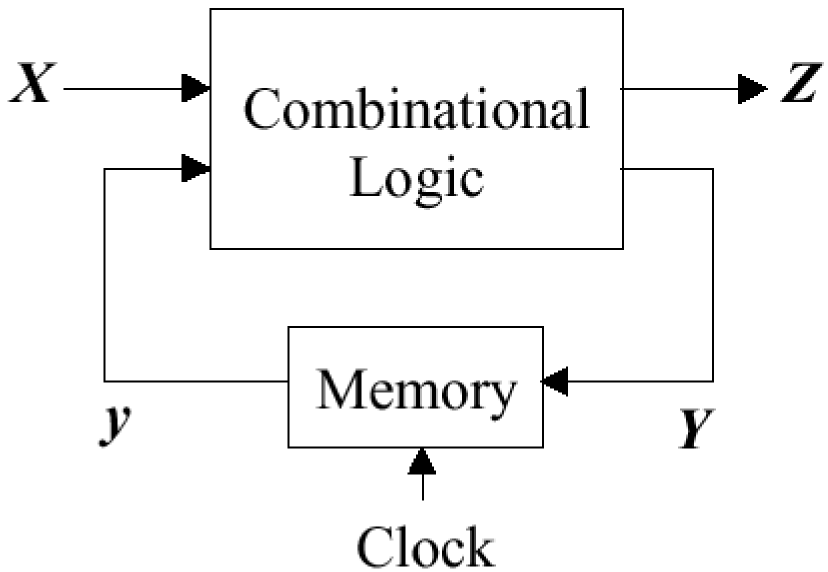


Fig. 5.3 General structure of a sequential logic circuit.

Asynchronous Sequential Circuit

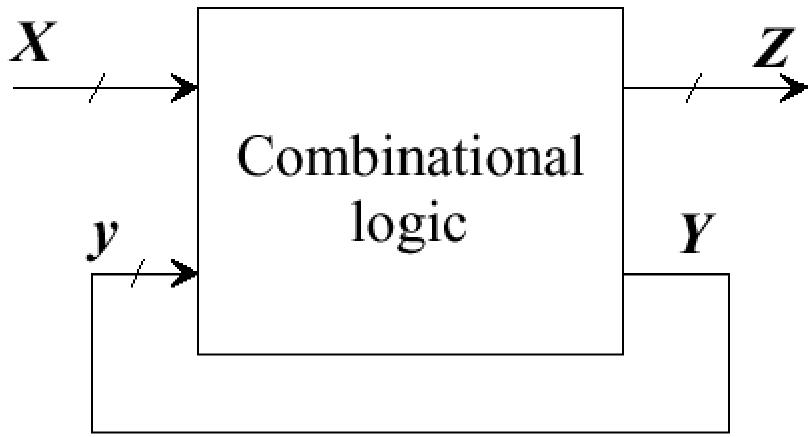


Fig. 5.4 General structure of an asynchronous sequential circuit.

Asynchronous Sequential Circuit

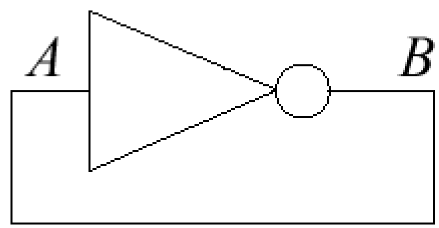


Fig. 5.5 Inverter connected into an asynchronous sequential logic circuit.

Oscillating Inverter

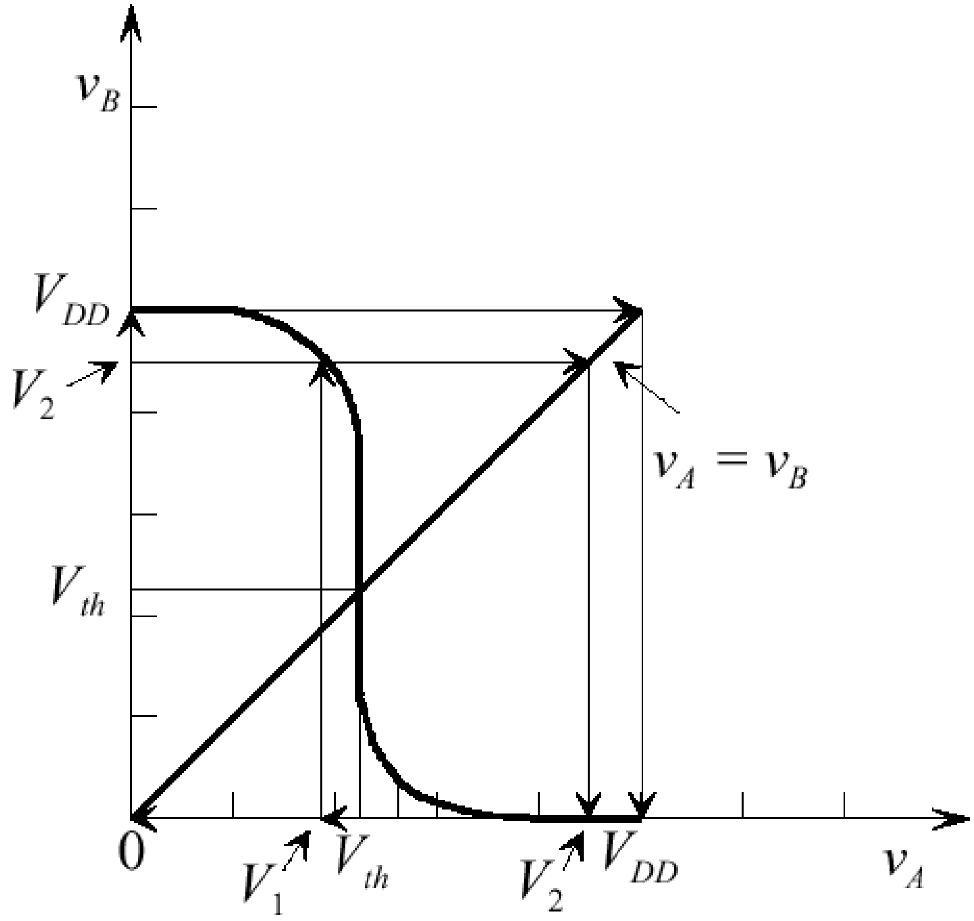


Fig. 5.6 Oscillation of an inverter with its output connected to its input.

Ring Oscillator

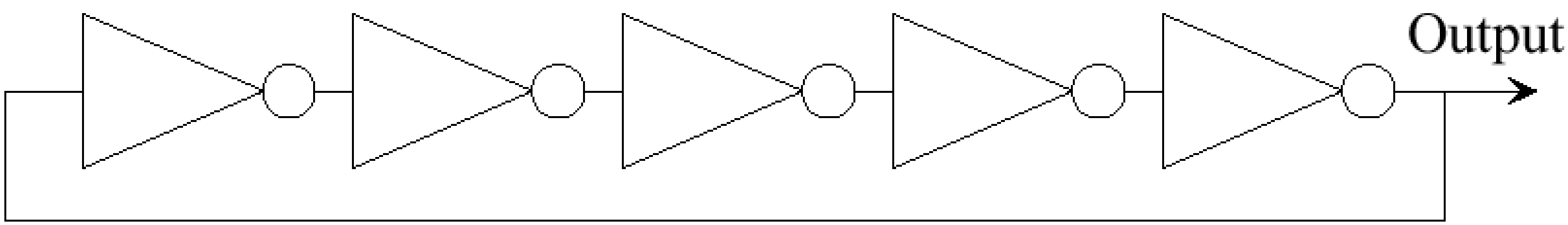


Fig. 5.7 Ring oscillator consisting of 5 inverters.

Inverter Loop

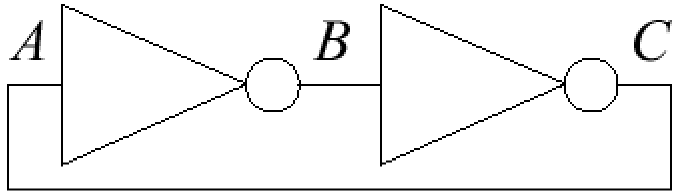


Fig. 5.8 Non-inverting loop formed by two inverters.

Operating Point

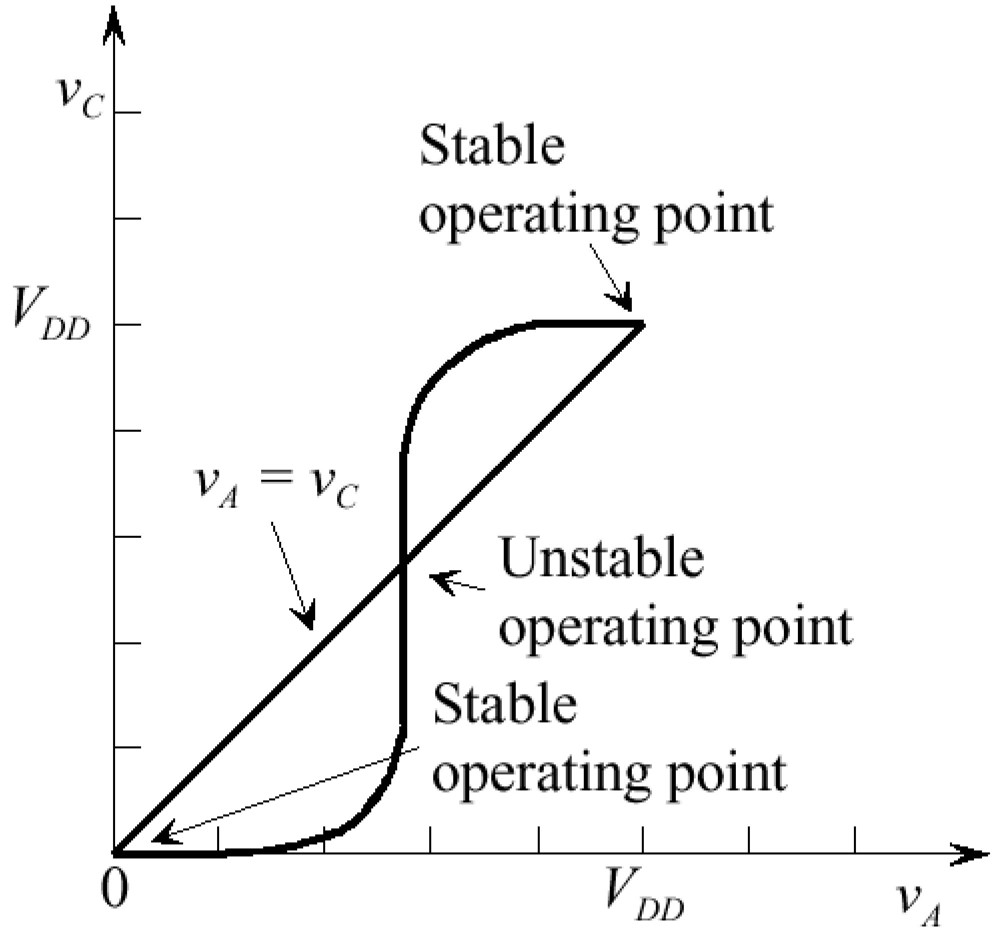


Fig. 5.9 Operating points of a CMOS memory element.

D-Latch

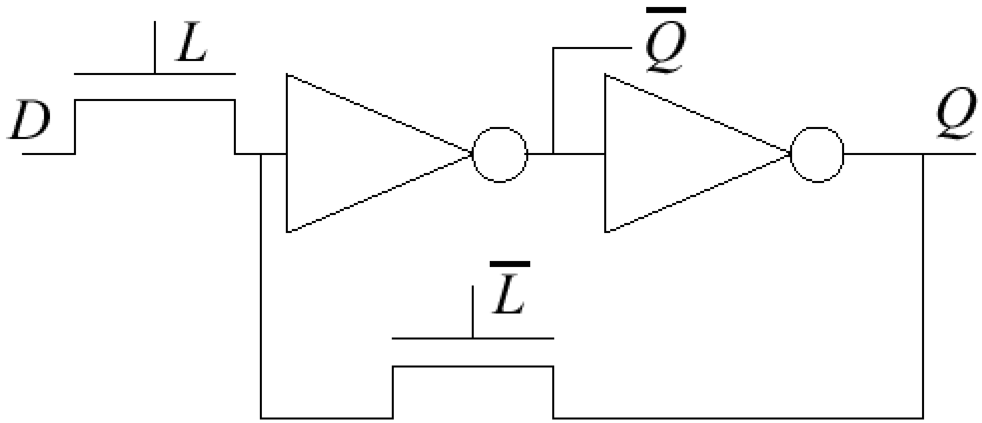


Fig. 5.10 A D-latch.

D-Latch

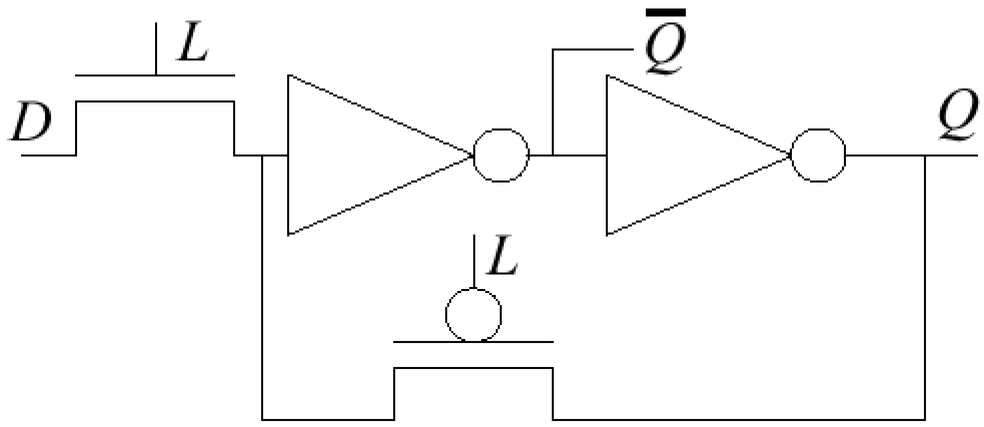


Fig. 5.11 An alternative D-latch utilizing a pMOS transistor.

D-Latch

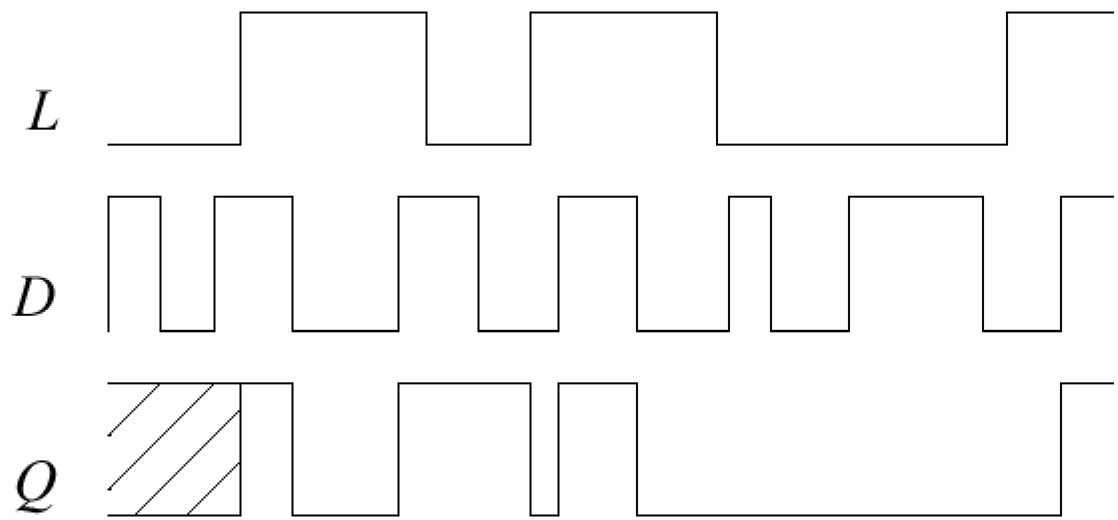


Fig. 5.12 Behavior of the D-latch.

Sequential Circuit

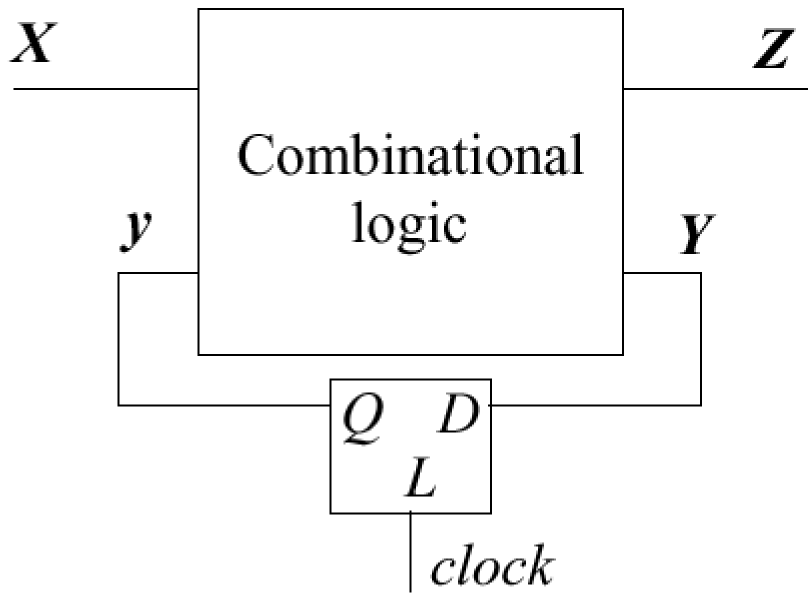


Fig. 5.13 Sequential logic circuit employing D-latches.

Clock

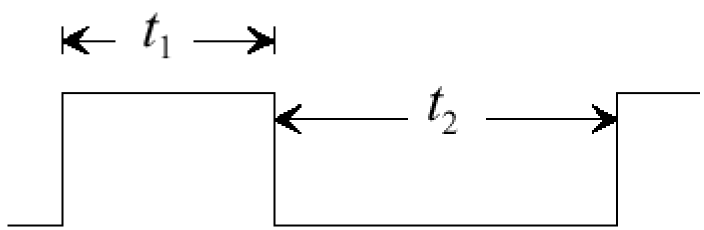


Fig. 5.14 Clock signal for the sequential logic circuit in Fig. 5.13.

Master-Slave FF

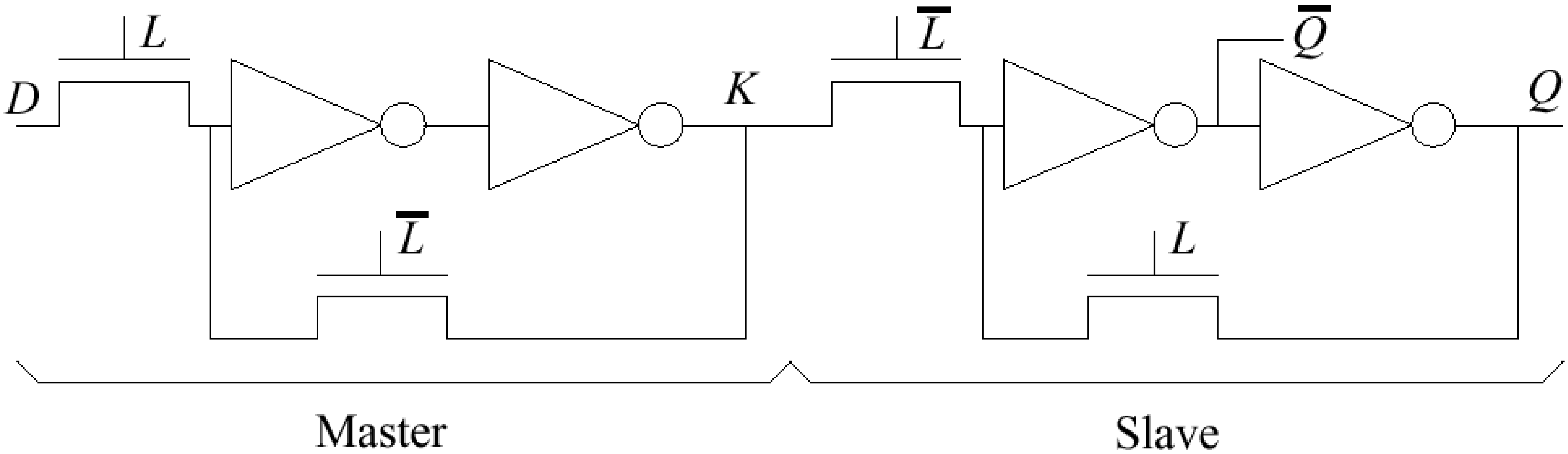


Fig. 5.15 Master-slave structure to form a D-flip-flop.

Negative-Edge-Triggered FF

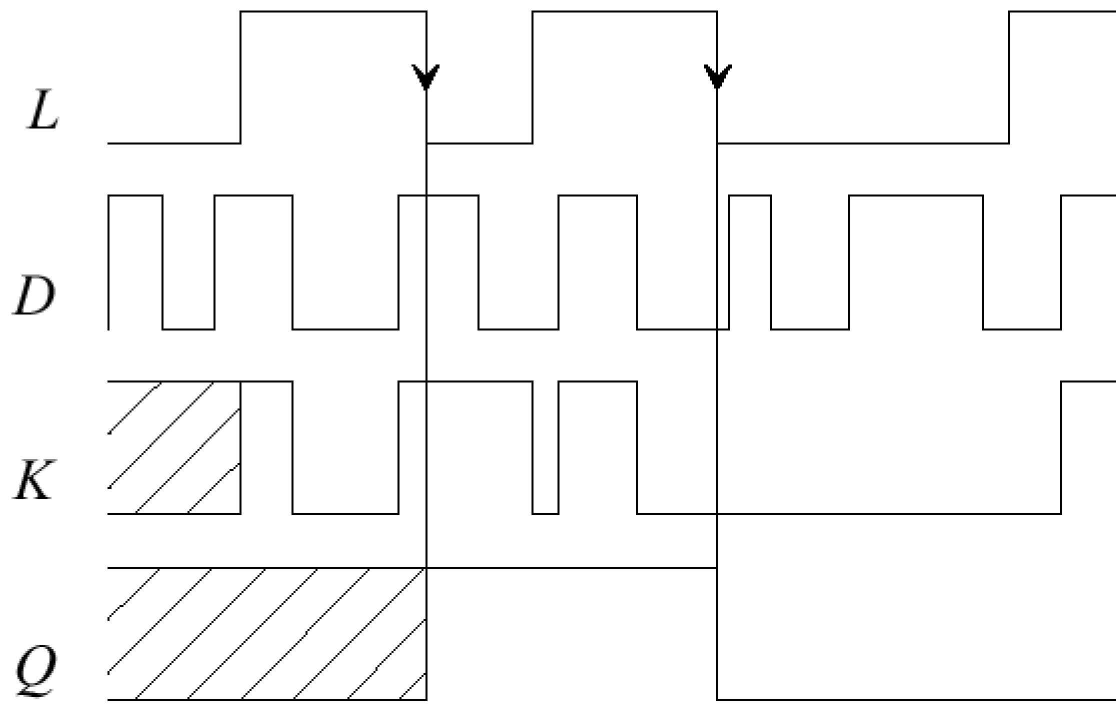
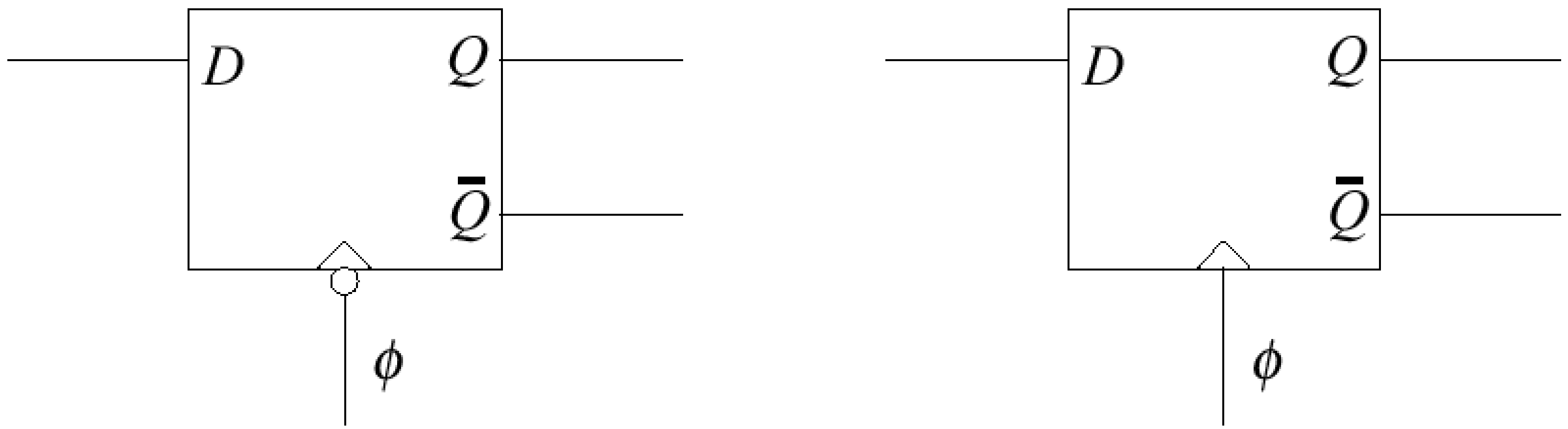


Fig. 5.16 Behavior of a negative-edge-triggered D-flip-flop.

Flip-Flops



Negative edge-triggered flip-flop   Positive edge-triggered flip-flop

Fig. 5.17 Symbols of flip-flops.

Sequential Circuit

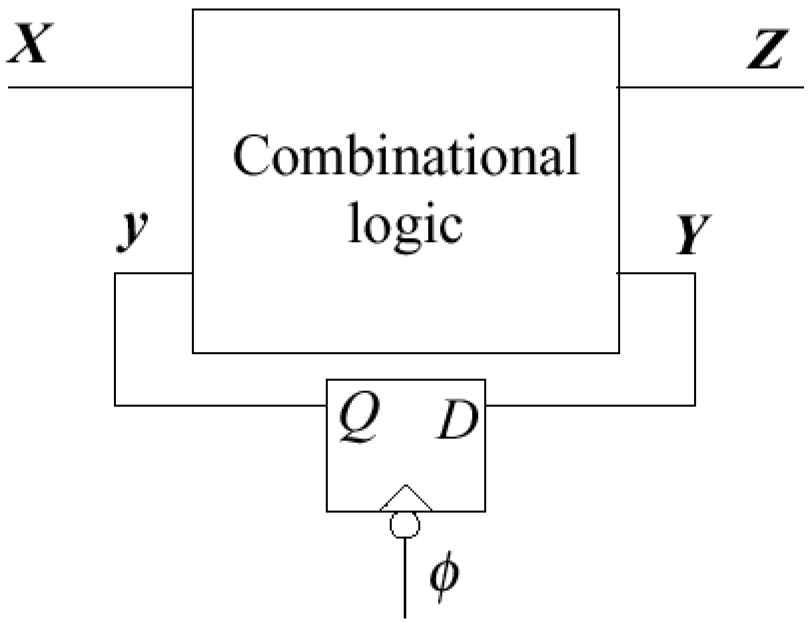


Fig. 5.18 Sequential circuit incorporating D-flip-flops.

Clock Design

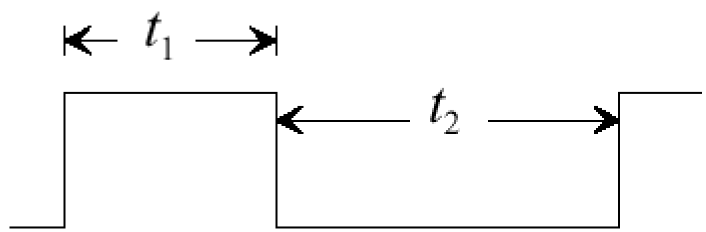


Fig. 5.19 Timing diagram for the design of an edge-triggering clock.

Sequential Circuit

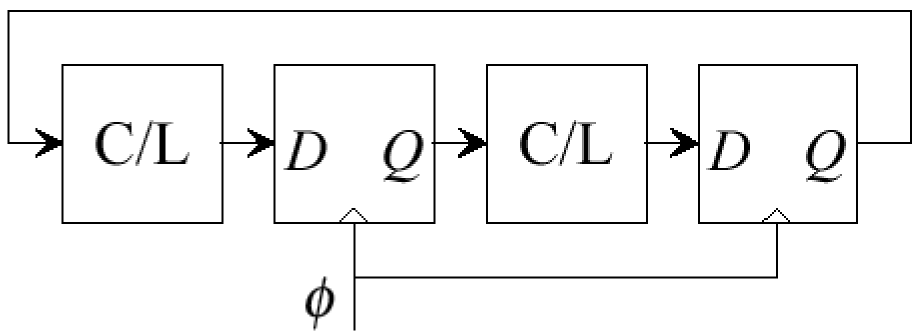


Fig. 5.20 Sequential circuit with two stages of combinational logic.

Two-Phase Non-Overlapping Clock

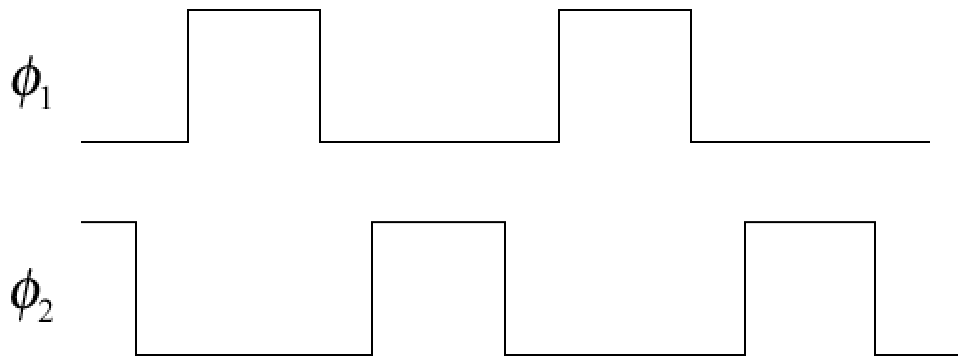


Fig. 5.21 Two-phase, non-overlapping clock signals.

Clock Overlapping

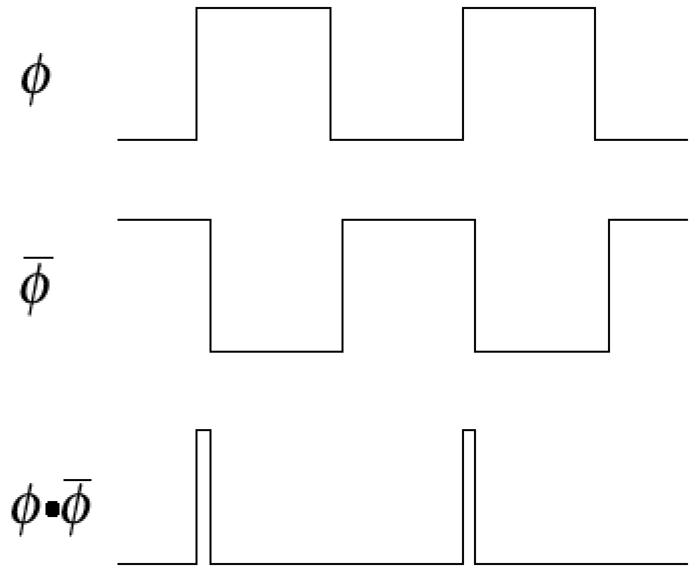


Fig. 5.22 Overlapping between ϕ and $\bar{\phi}$.

Stable Signal

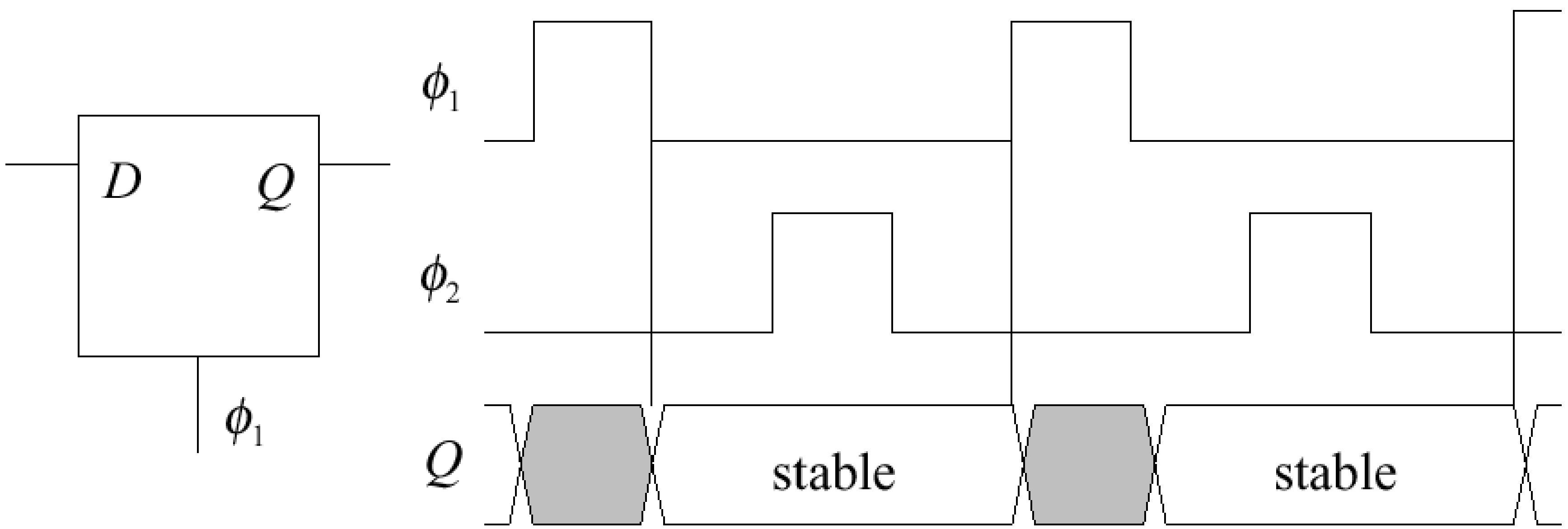


Fig. 5.23 Output Q of a latch controlled by ϕ_1.

Clock Signal Assignment

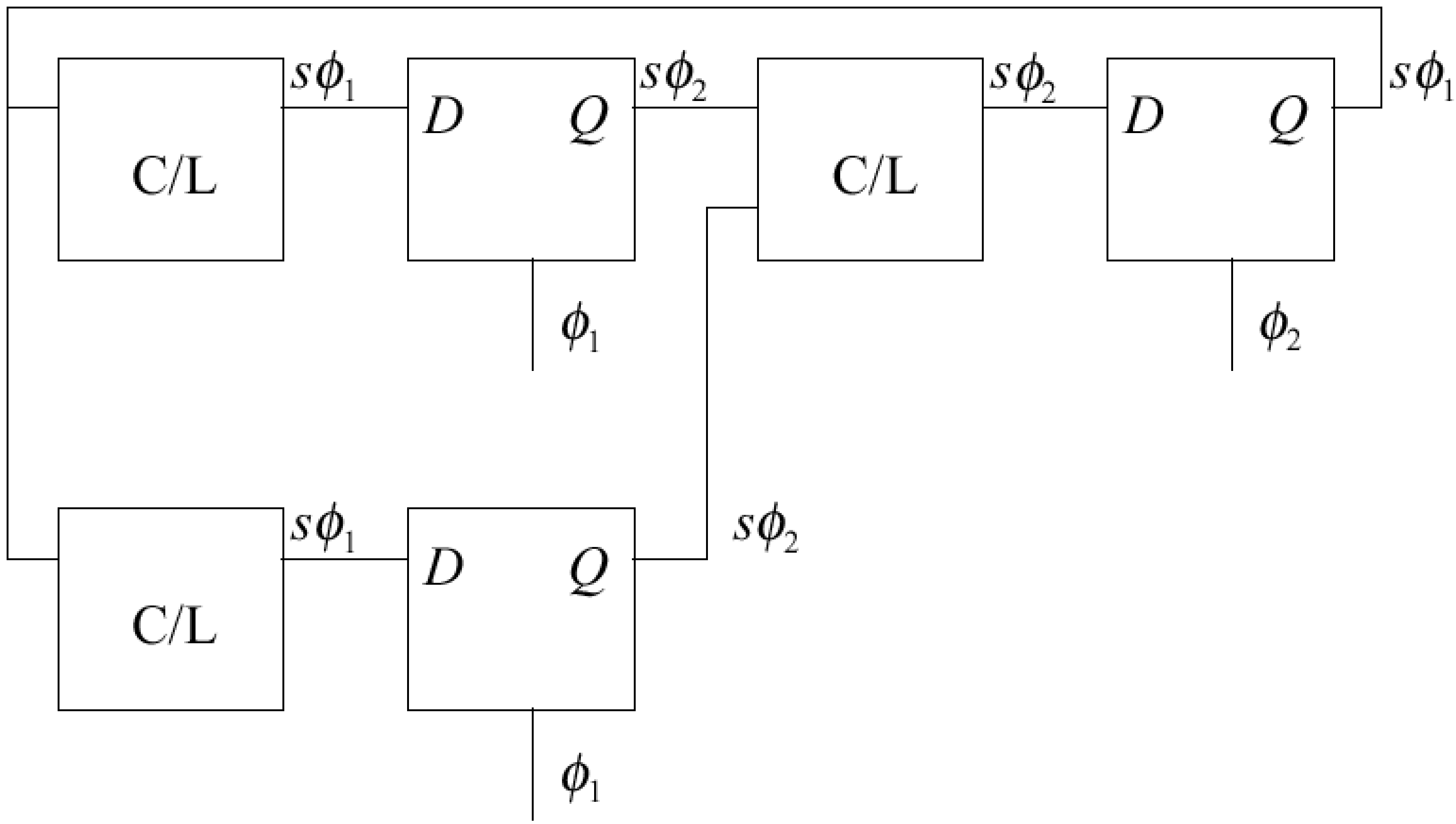


Fig. 5.24 Assignment of clock signals.

Two-Phase Non-Overlapping Clock

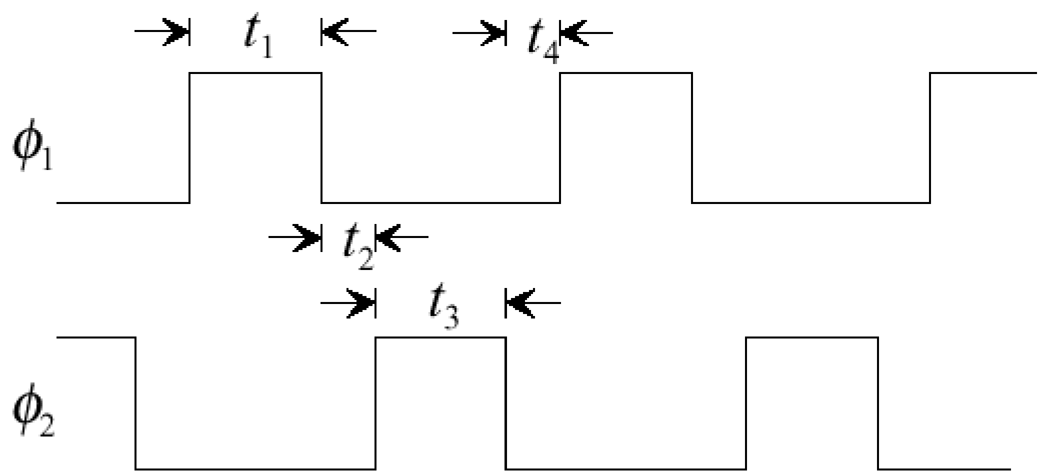


Fig. 5.25 Design of a two-phase, non-overlapping clock system.

Retiming

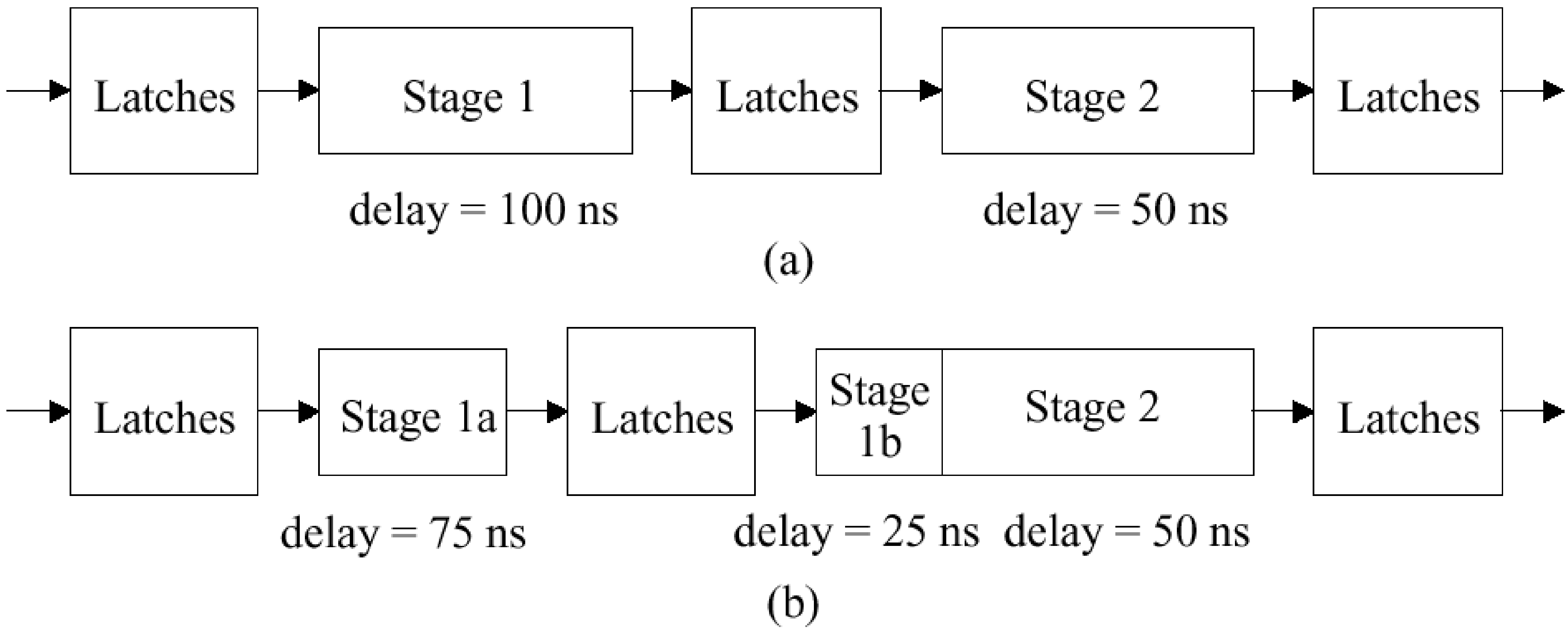


Fig. 5.26 Retiming example.

Clock Routing

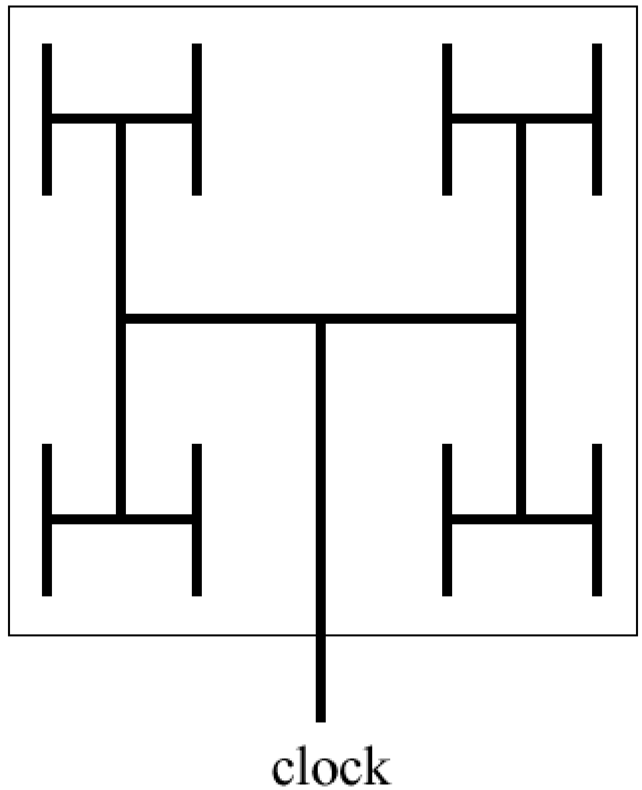


Fig. 5.27 H-tree clock routing scheme.

Robot Lawn Mower

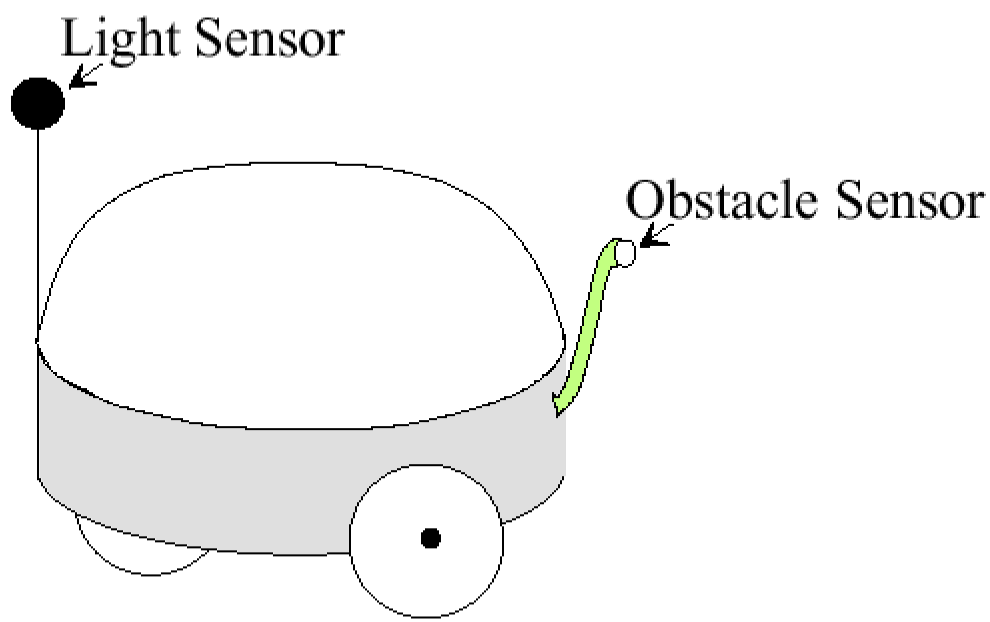


Fig. 5.28 Illustration of the robot lawn mower.

Mobile Robot

Sensor	Signal	Meaning	
Light	x	0: dark	1: bright
Obstacle	y	0: obstacle free	1: obstacle detected

Fig. 5.29 The sensor signals and their meanings.

Mobile Robot

pq	Left motor	Right motor	Robot
00	off	off	stops
01	off	on	turns left
10	on	off	turns right
11	on	on	goes straight

Fig. 5.30 Relations between control signals and robot movements.

Mobile Robot

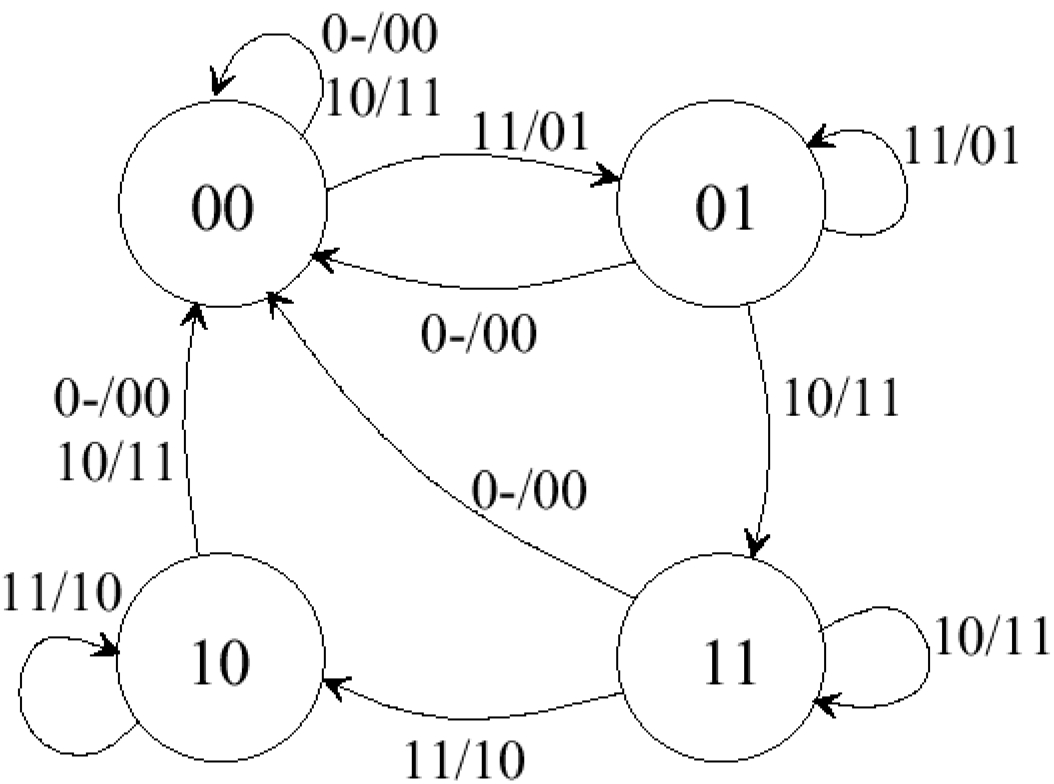


Fig. 5.31 Mealy machine state diagram for the mobile robot controller.

Mobile Robot

State	Meaning
00	Next obstacle will be avoided by turning left
01	Turning left
11	Next obstacle will be avoided by turning right
10	Turning right

Fig. 5.32 States of the mobile robot controller.

Mobile Robot

s_1s_0	xy = 0- S_1S_0pq	xy = 10 S_1S_0pq	xy = 11 S_1S_0pq
00	0000	0011	0101
01	0000	1111	0101
11	0000	1111	1010
10	0000	0011	1010

Fig. 5.33 State table for the mobile robot controller.

Mobile Robot

S_1 xy / s_1s_0	00	01	11	10
00	0	0	0	0
01	0	0	0	1
11	0	0	1	1
10	0	0	1	0

S_0 xy / s_1s_0	00	01	11	10
00	0	0	1	0
01	0	0	1	1
11	0	0	0	1
10	0	0	0	0

p xy / s_1s_0	00	01	11	10
00	0	0	0	1
01	0	0	0	1
11	0	0	1	1
10	0	0	1	1

q xy / s_1s_0	00	01	11	10
00	0	0	1	1
01	0	0	1	1
11	0	0	0	1
10	0	0	0	1

Fig. 5.34 Knaugh maps for mobile robot controller design.

Mobile Robot

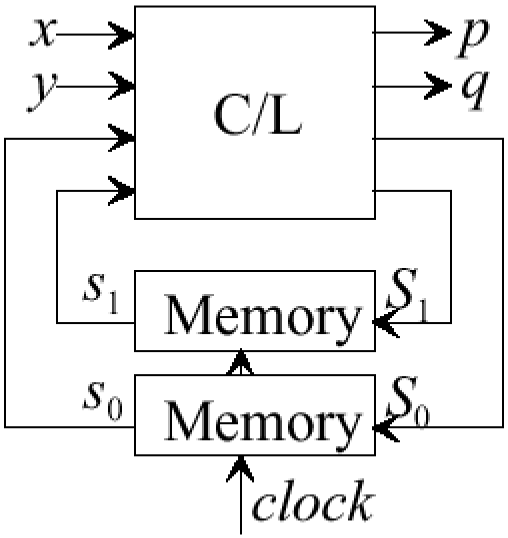


Fig. 5.35 Block diagram for the mobile robot controller circuit.

64-Bit Adder

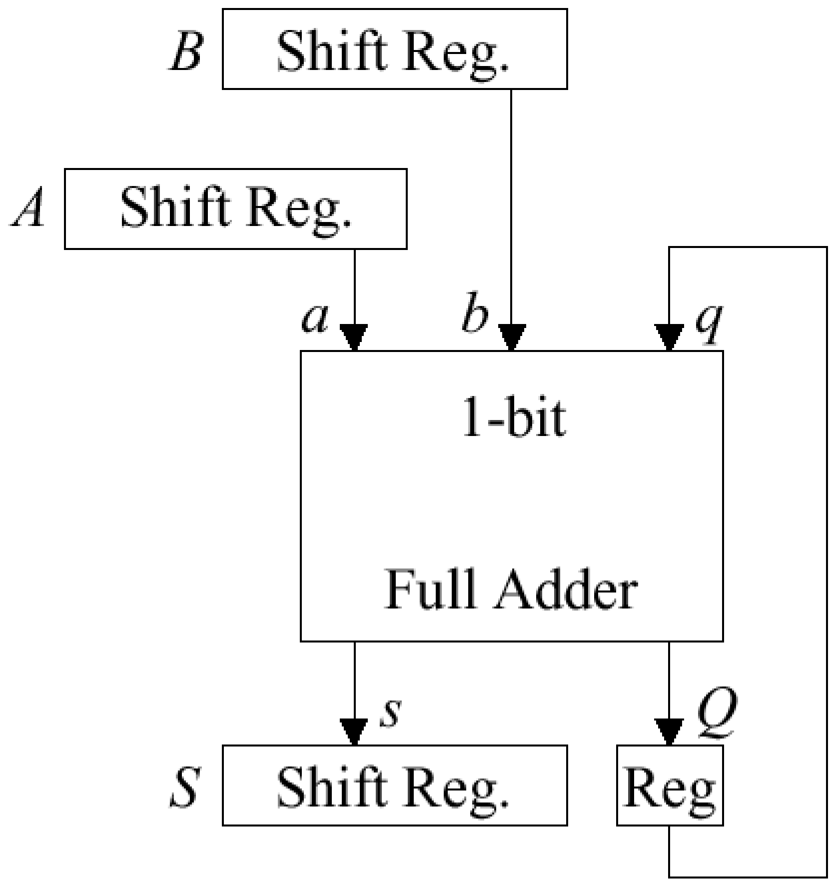


Fig. 5.36 64-bit adder.

Candy Machine

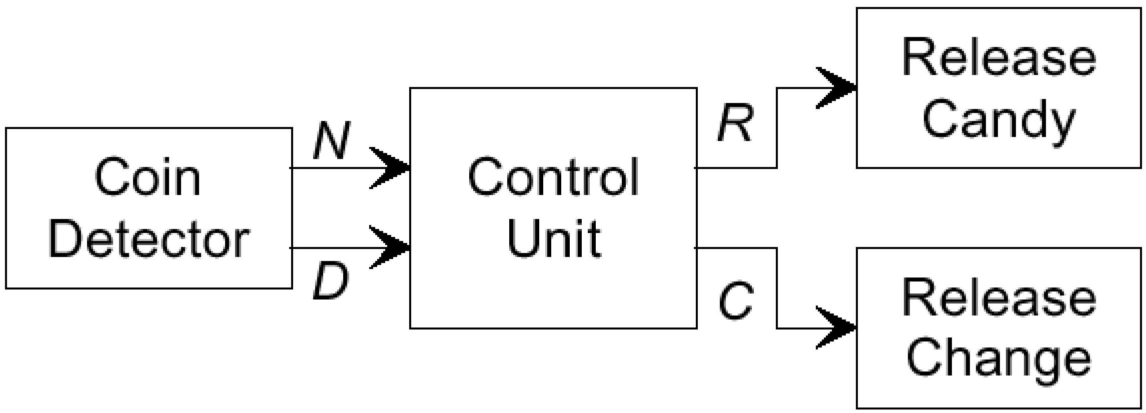


Fig. 5.37 Block diagram of a candy machine.

Candy Machine

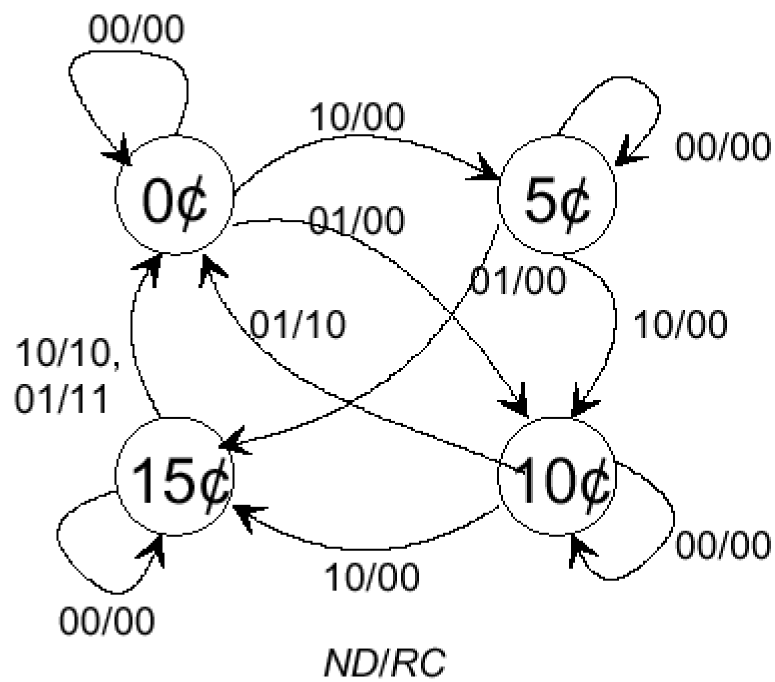


Fig. 5.38 State diagram for a candy machine.