Chapter 3

IC Layout and Fabrication

Silicon Wafer

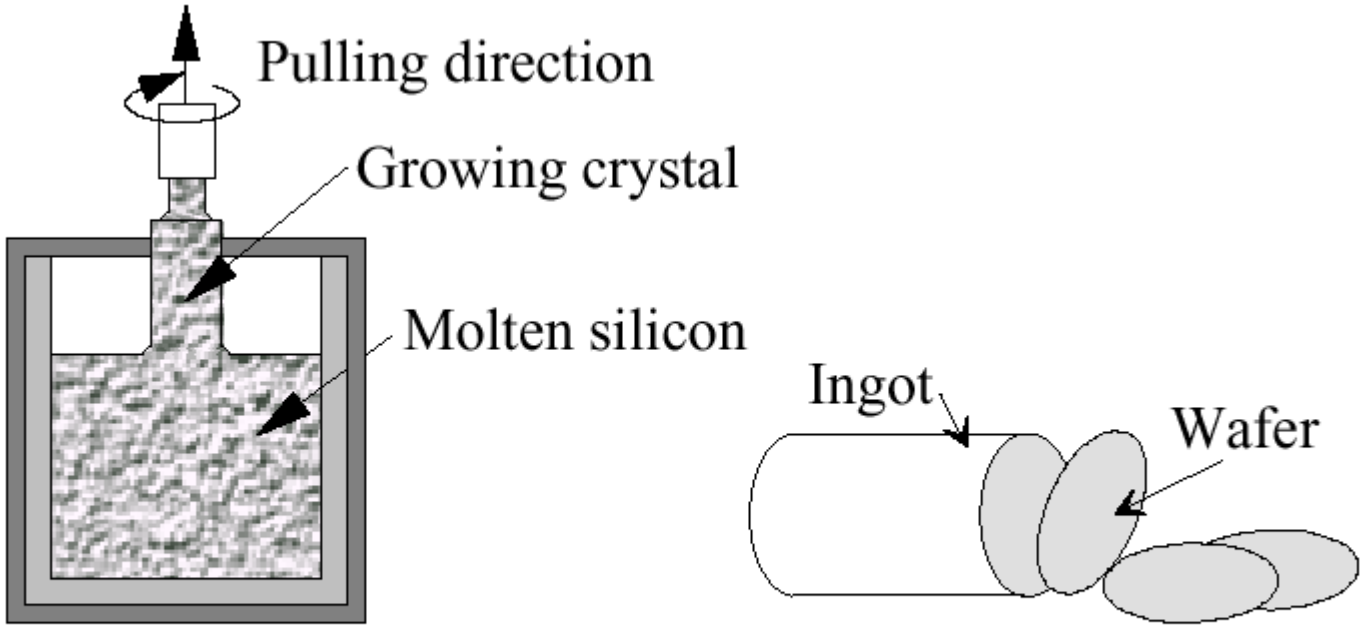
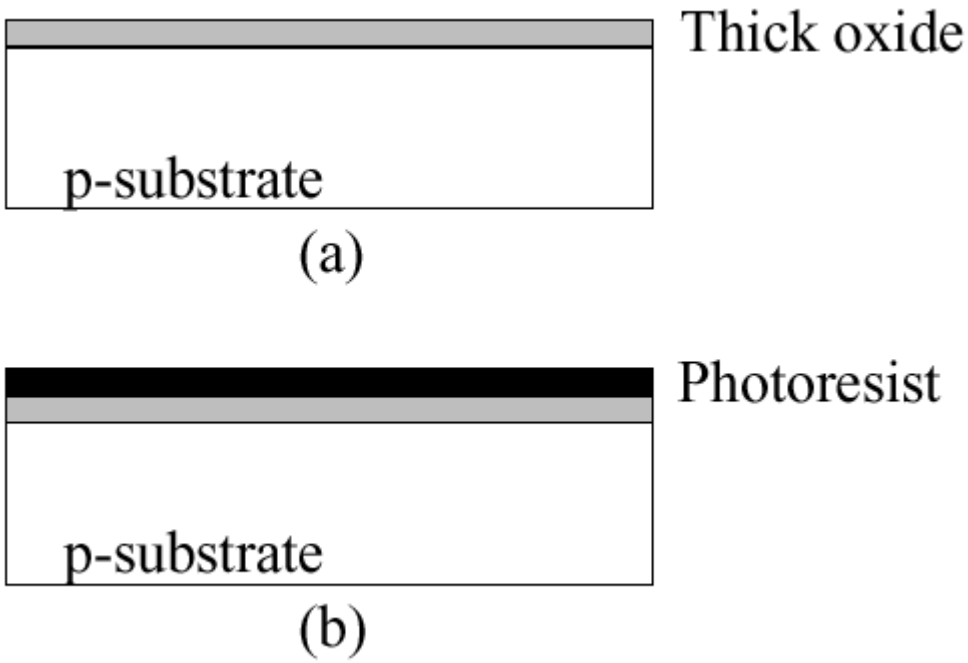
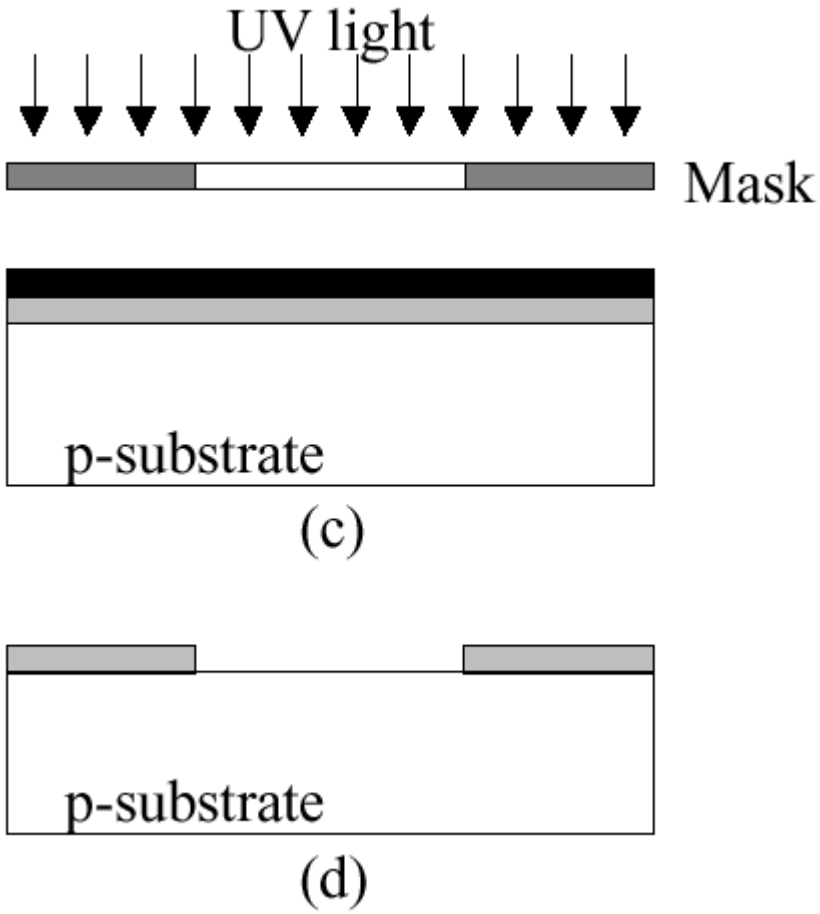


Fig. 3.1 Silicon wafer manufacturing process.

Doping



Doping



Doping

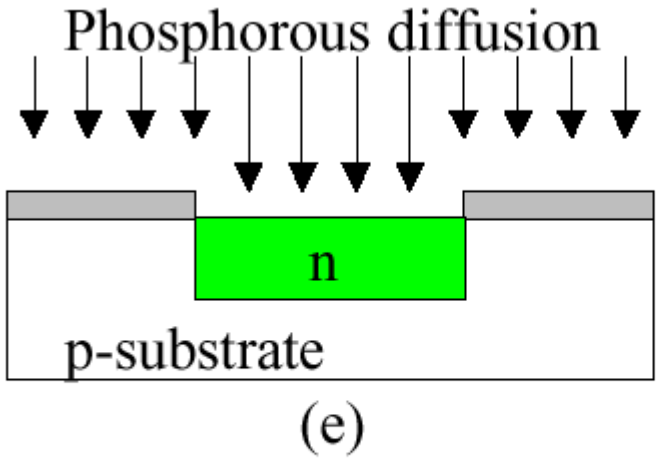
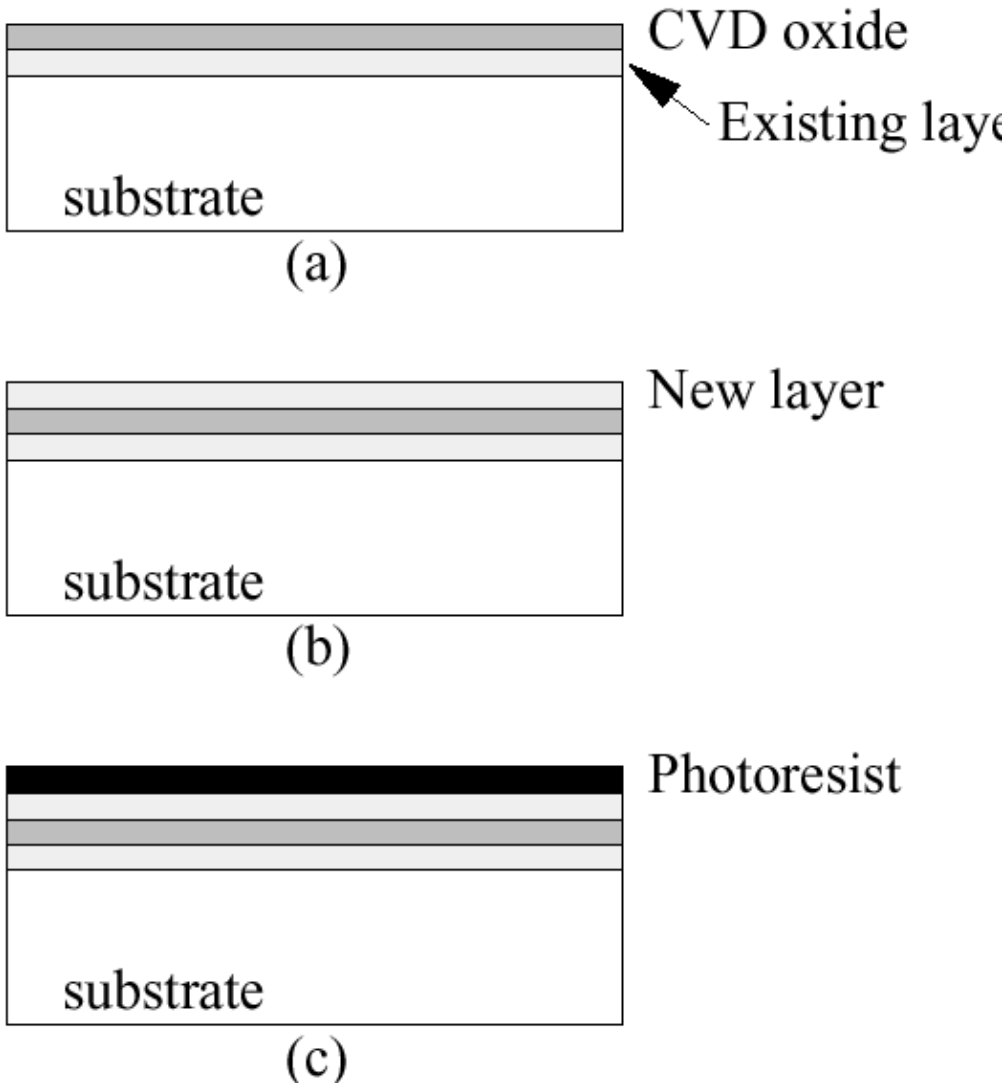
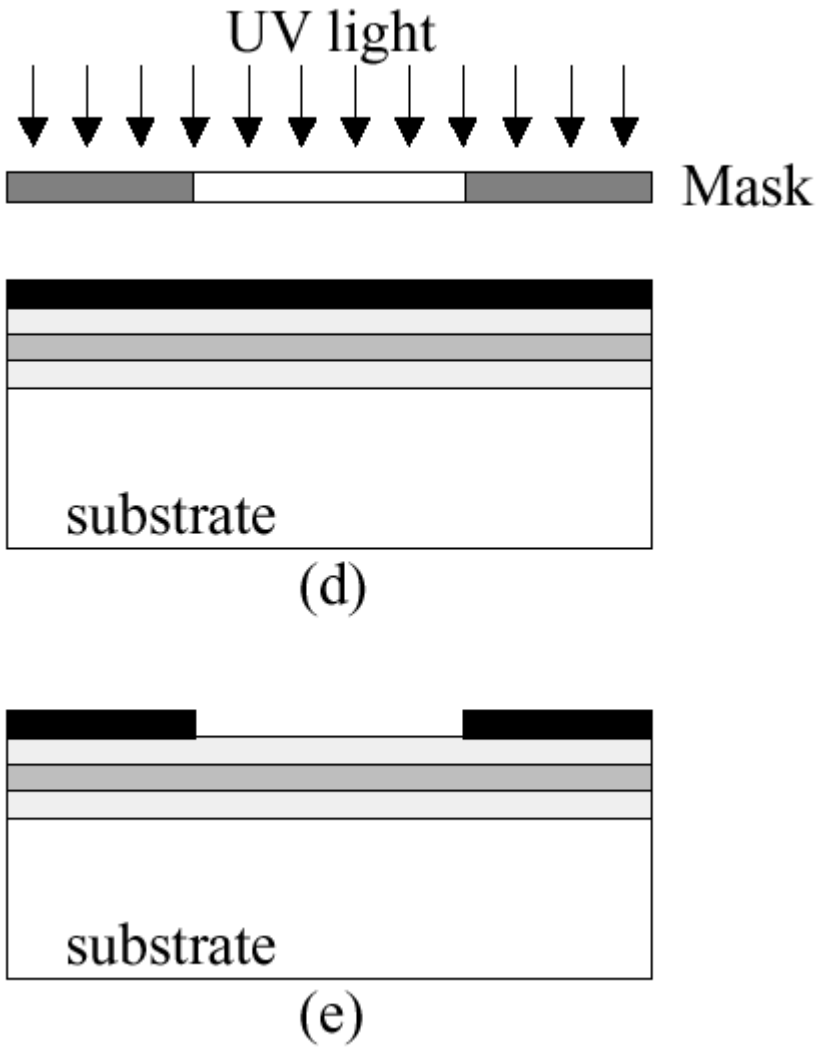


Fig. 3.2 Doping to a selected wafer region.

Top Layers



Top Layers



Top Layers

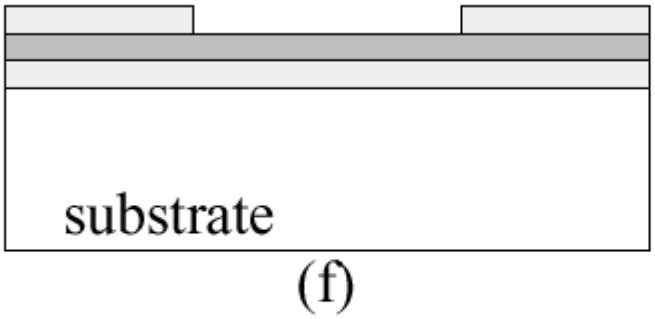


Fig. 3.3 Creating layers on top of the wafer.

Inverter

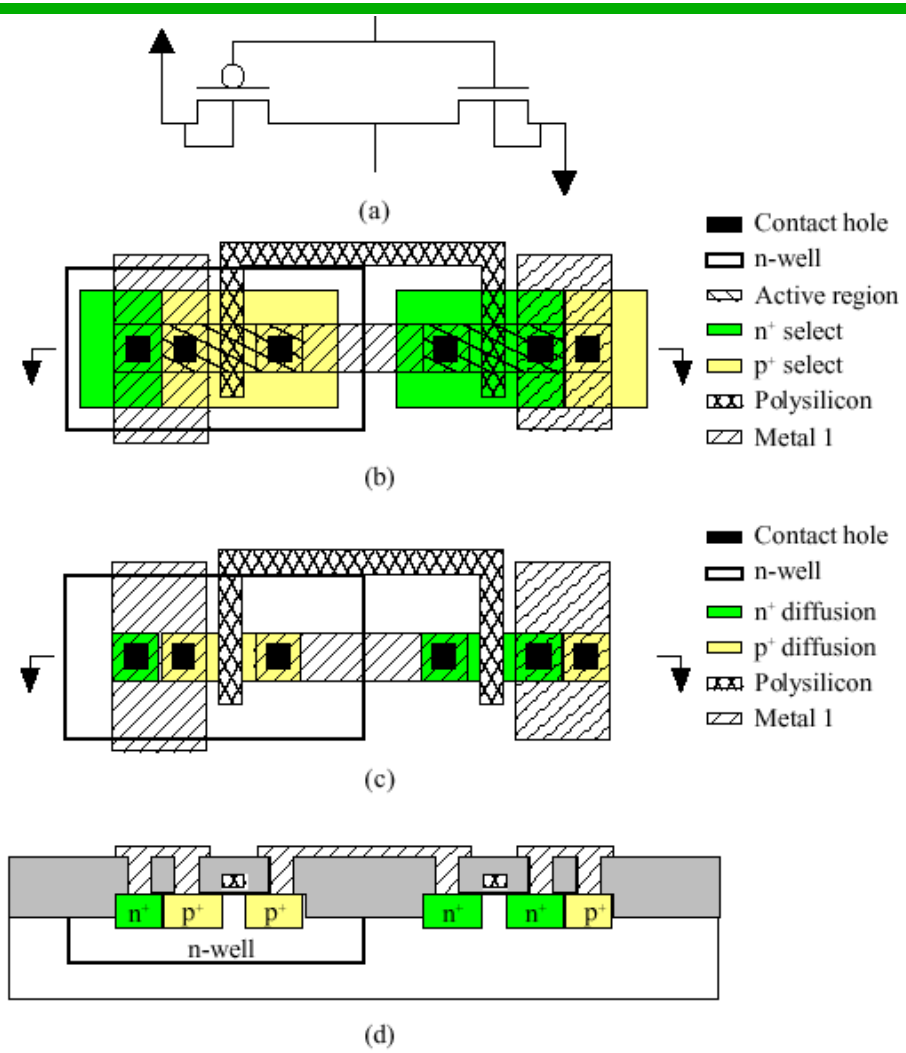


Fig. 3.4 CMOS inverter: (a) transistor schematic; (b) composite layout; (c) top view; (d) cross sectional view.

N-Well

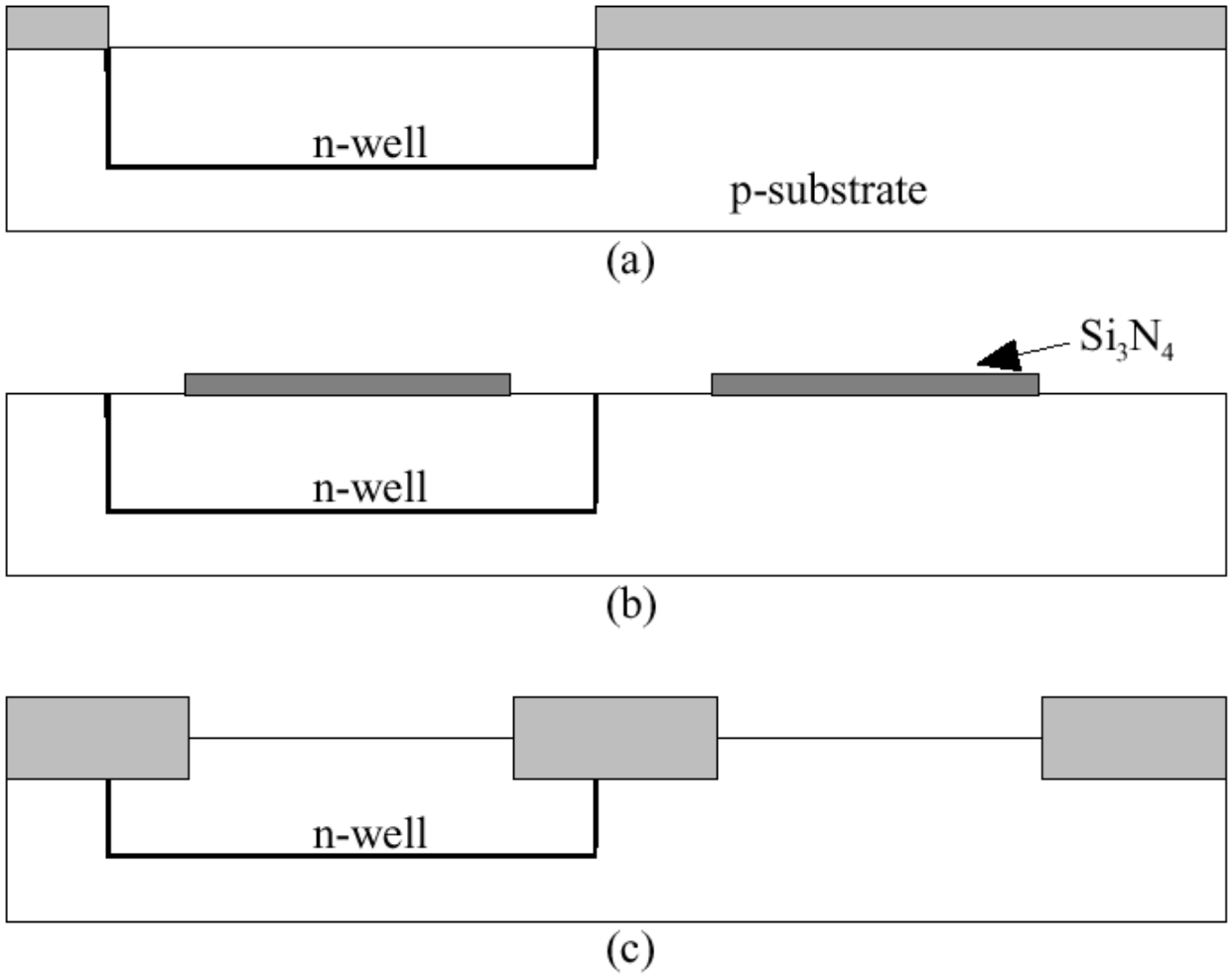
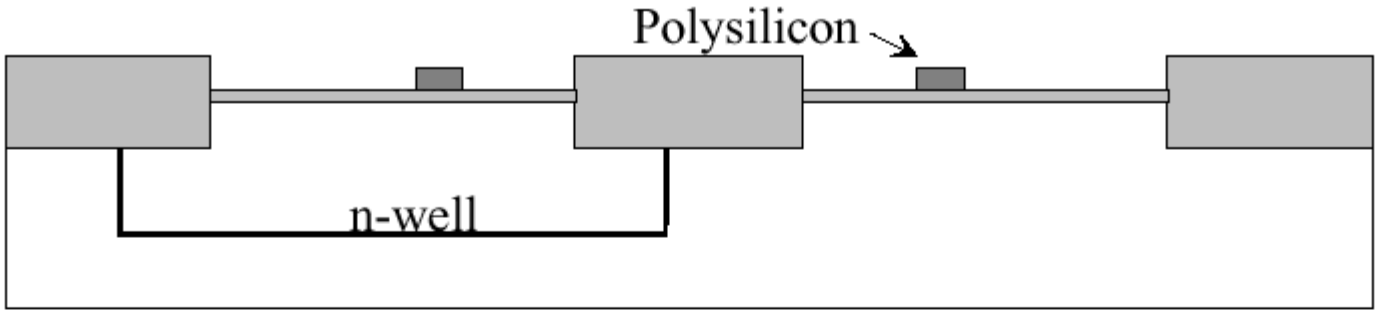
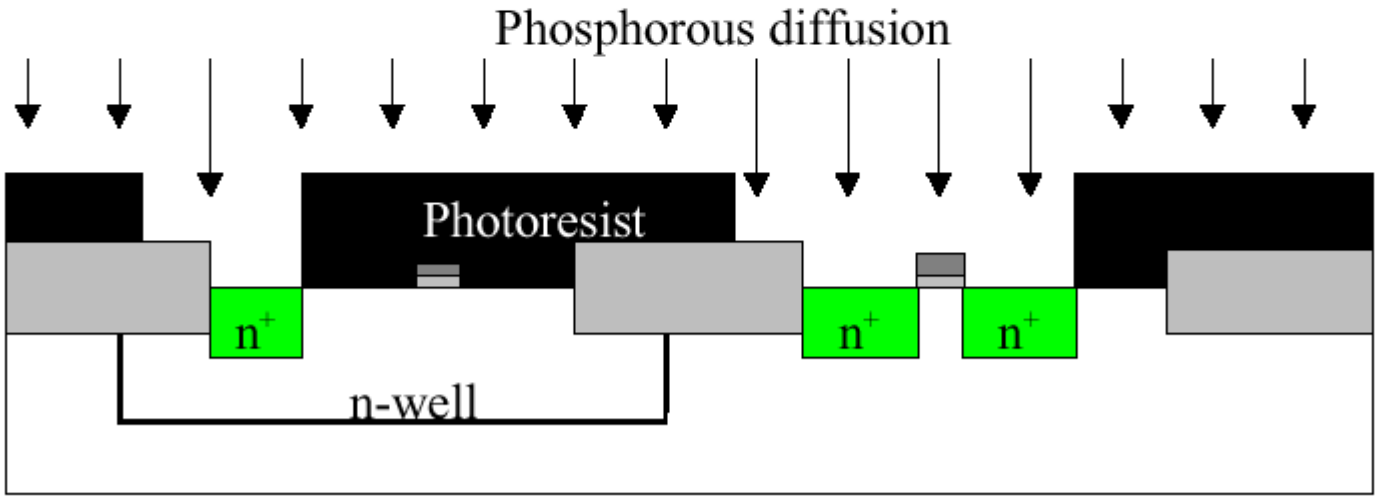


Fig. 3.5 Creating an n-well for CMOS circuits.

Self-Aligned Process



(a)



(b)

Self-Aligned Process

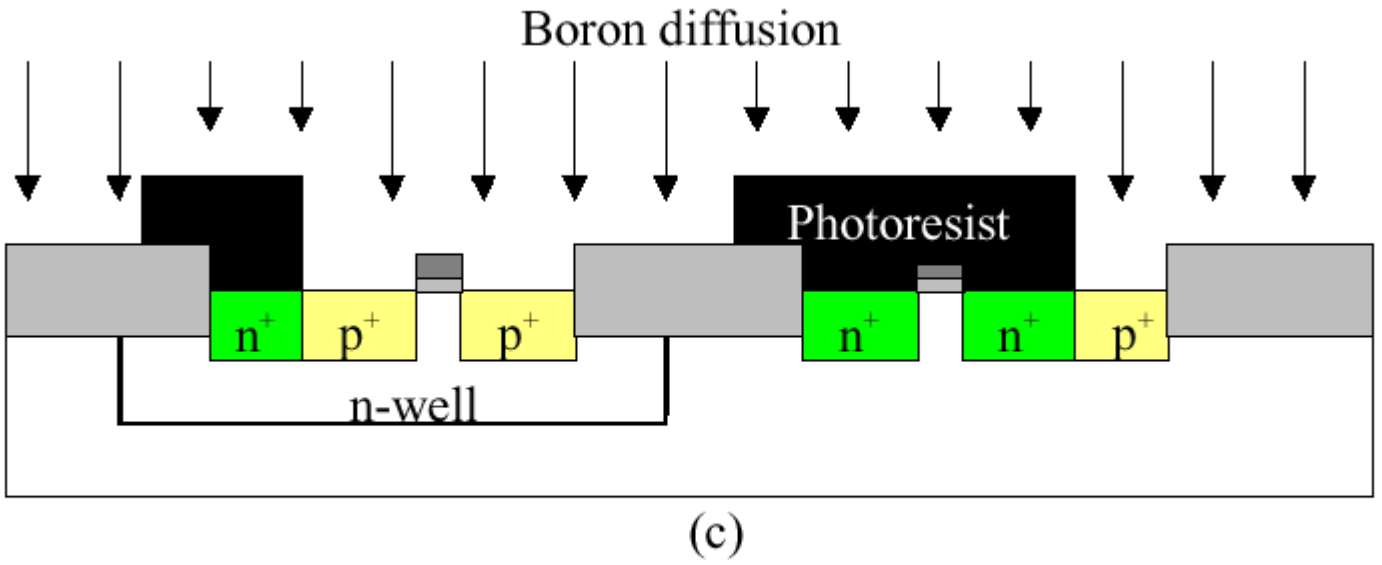


Fig. 3.6 Self-aligned process of creating transistors for the inverter.

Metallization

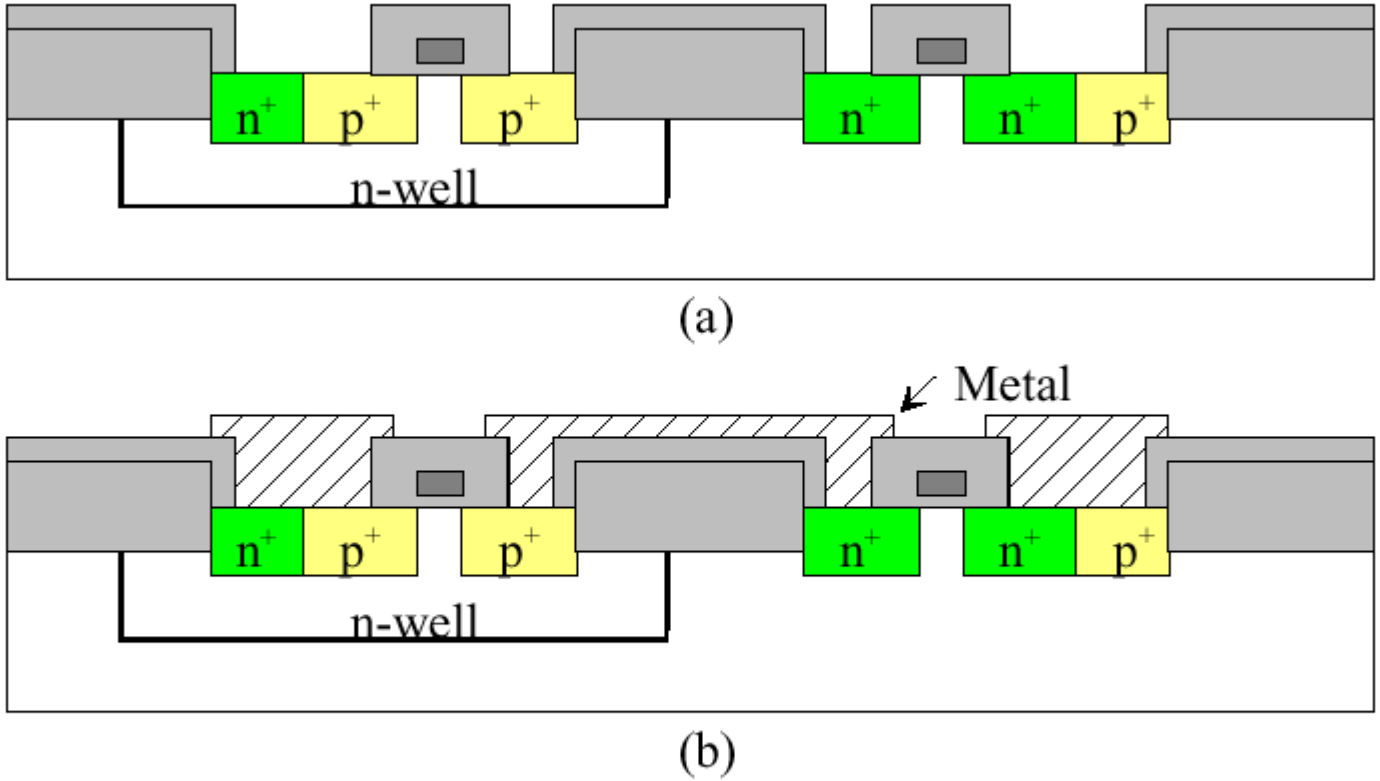


Fig. 3.7 Metallization process of a CMOS inverter.

Transistor and Layouts

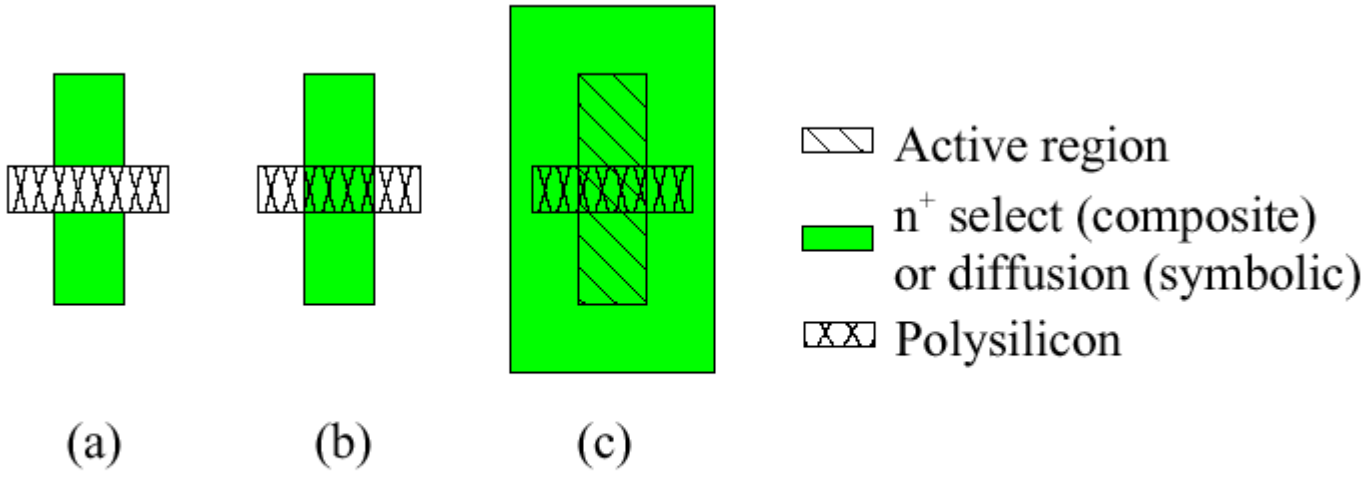


Fig. 3.8 Relationship between a physical transistor and its layouts.

Mask Layer Legends

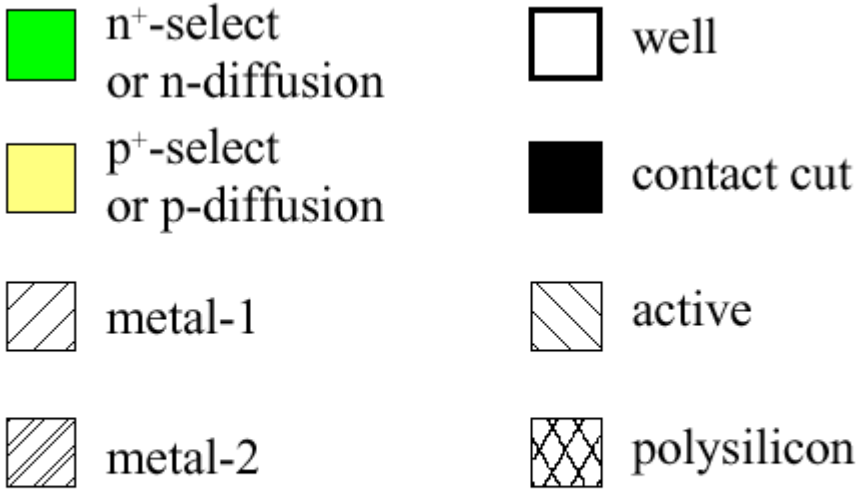


Fig. 3.9 Legends for different IC mask layers.

Polysilicon Design Rules

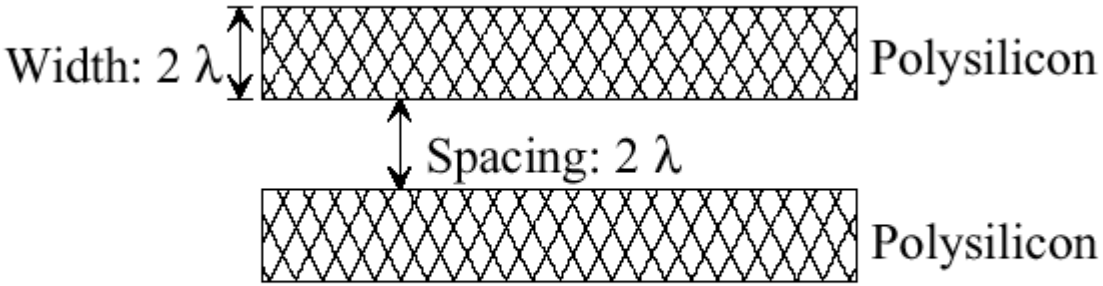


Fig. 3.10 Polysilicon design rules.

Diffusion Design Rules

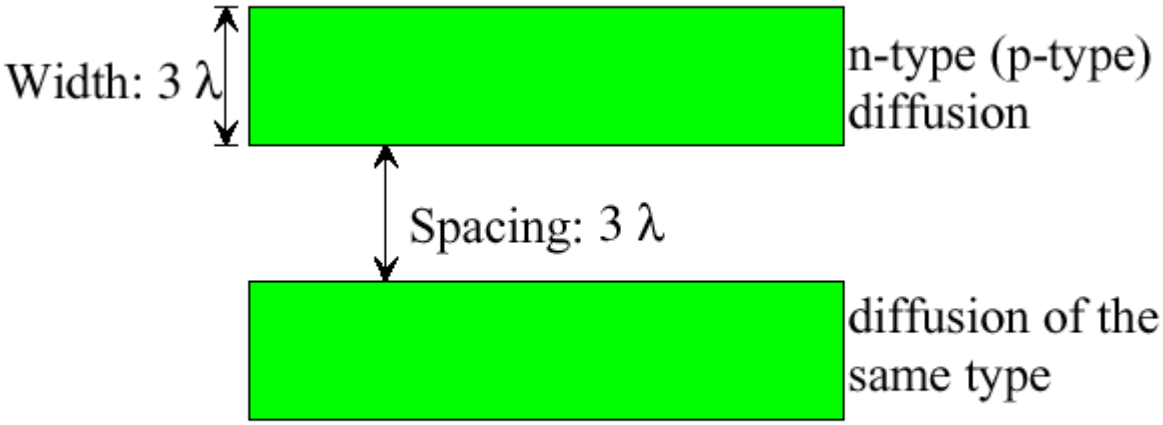


Fig. 3.11 Diffusion (n-type or p-type) design rules.

Diffusion Design Rules

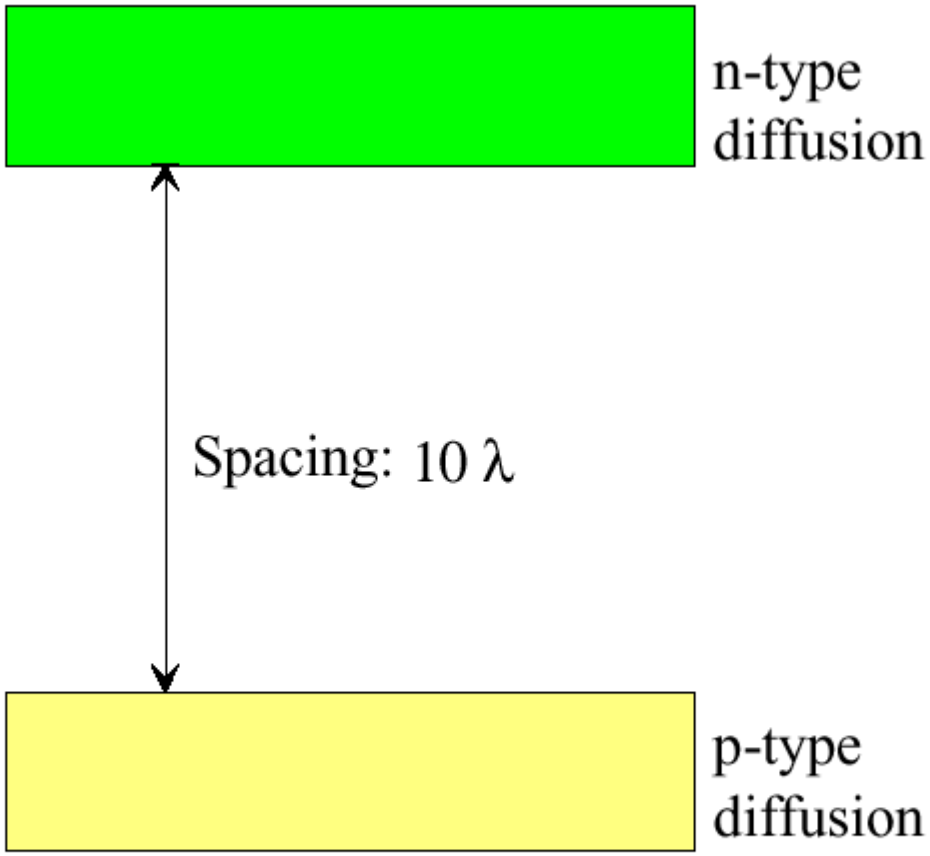


Fig. 3.12 Spacing between different types of diffusion.

Transistor Design Rules

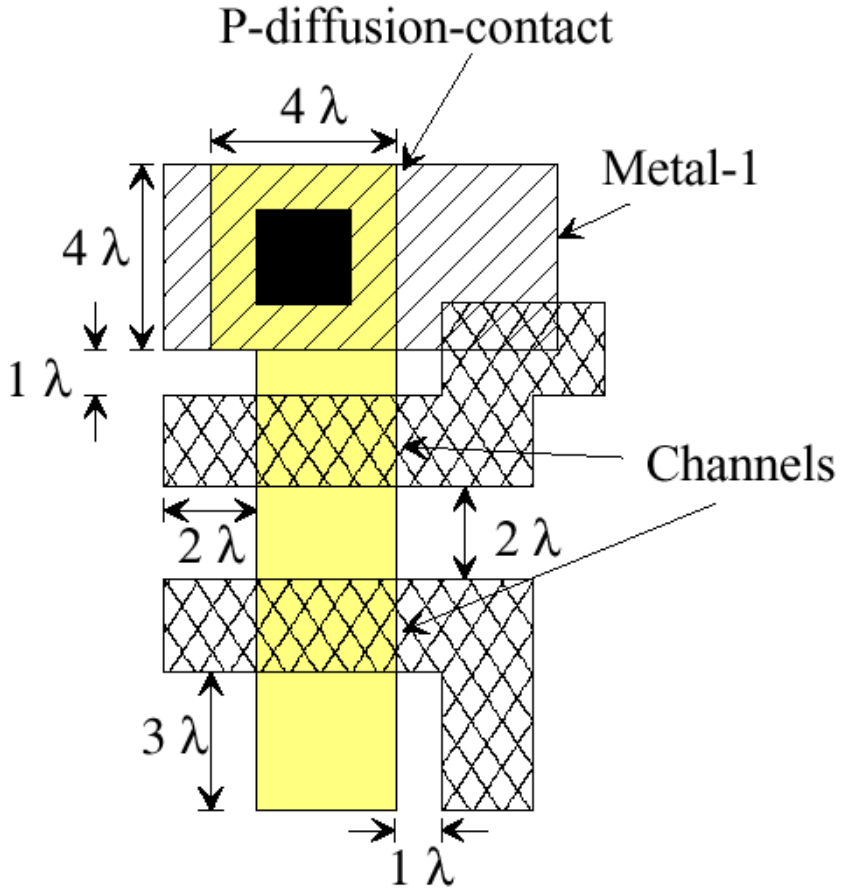


Fig. 3.13 Transistor (symbolic) design rules.

N-Well Design Rules

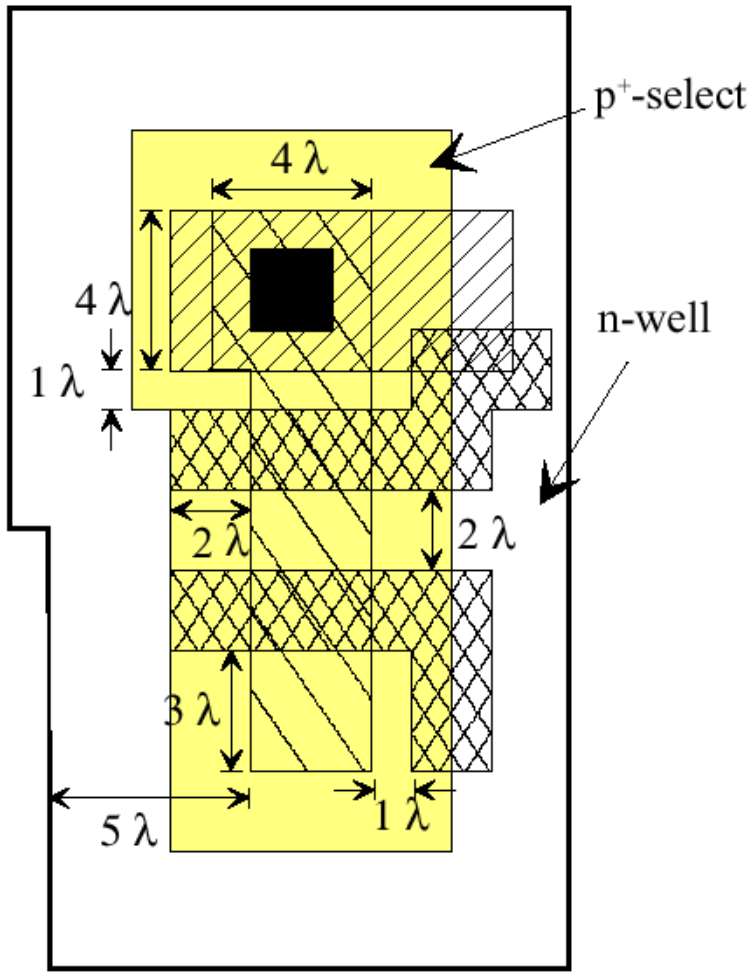


Fig. 3.14 Select area and n-well design rules.

Metal-1 Design Rules

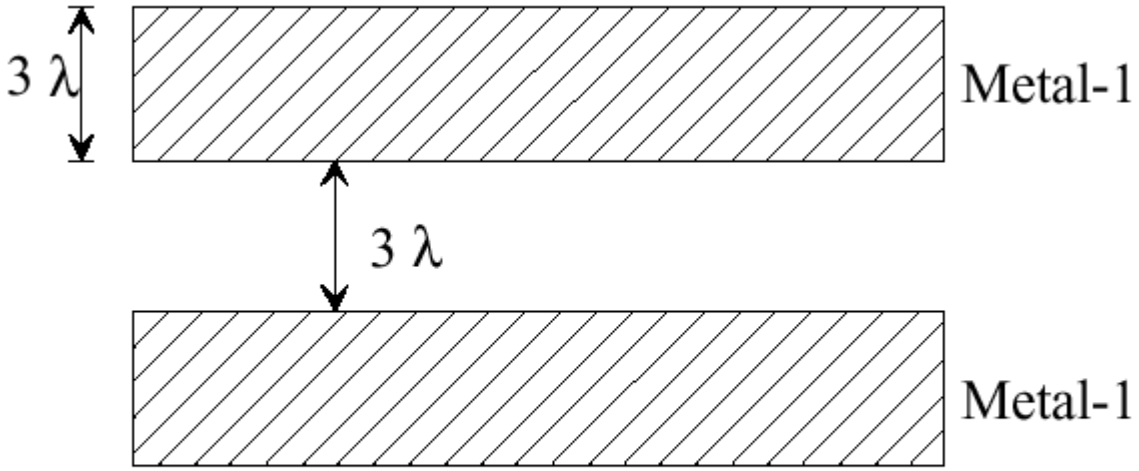


Fig. 3.15 Metal-1 design rules.

Metal-2 Design Rules

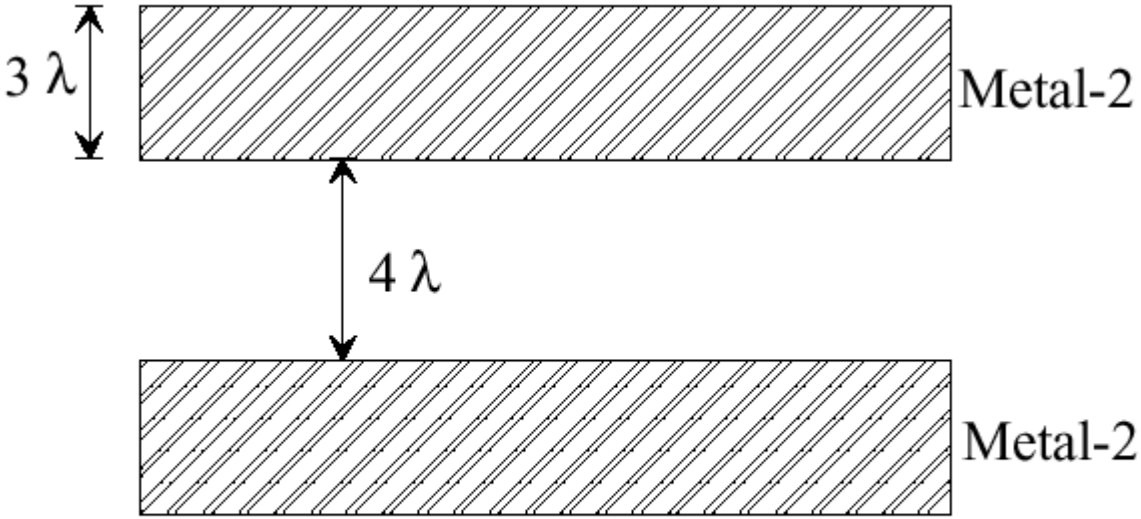
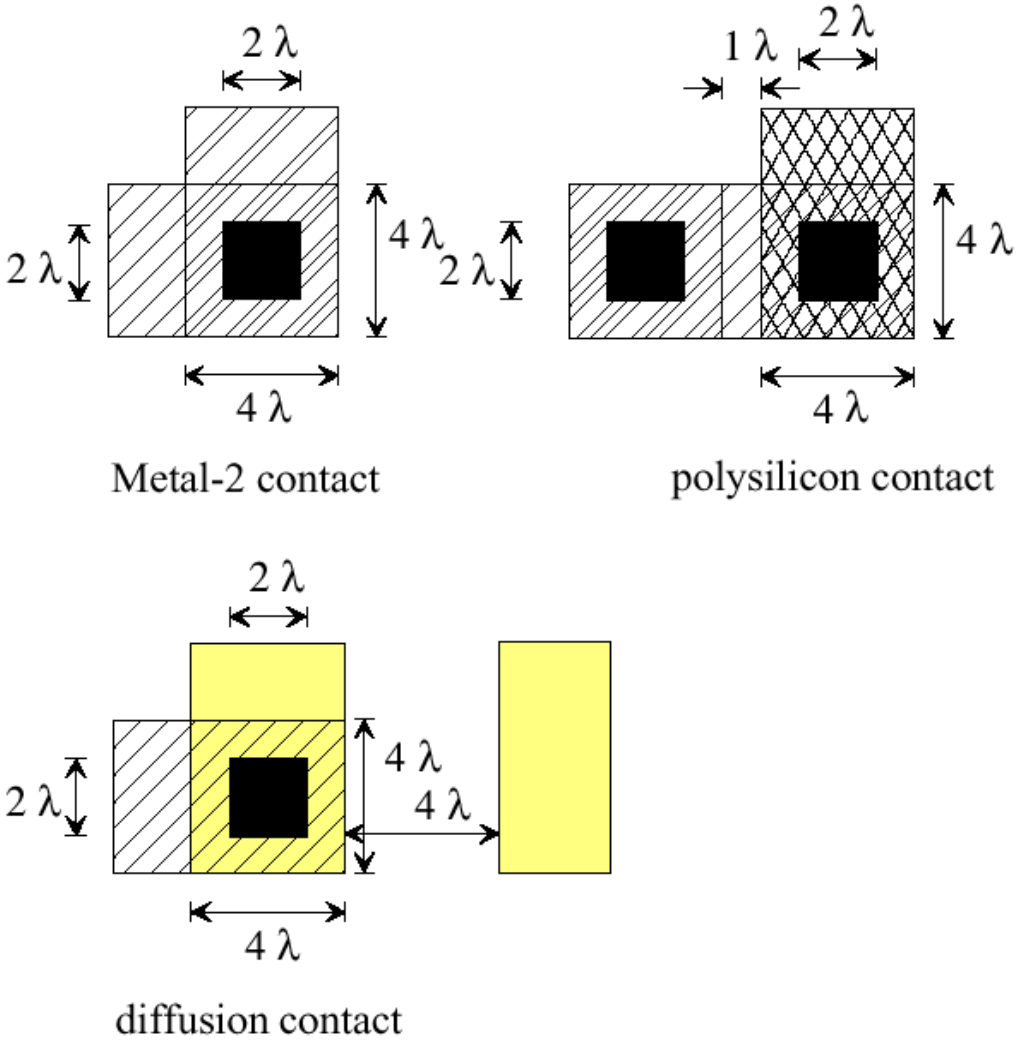


Fig. 3.16 Metal-2 design rules.

Contact Design Rules



Contact Design Rules

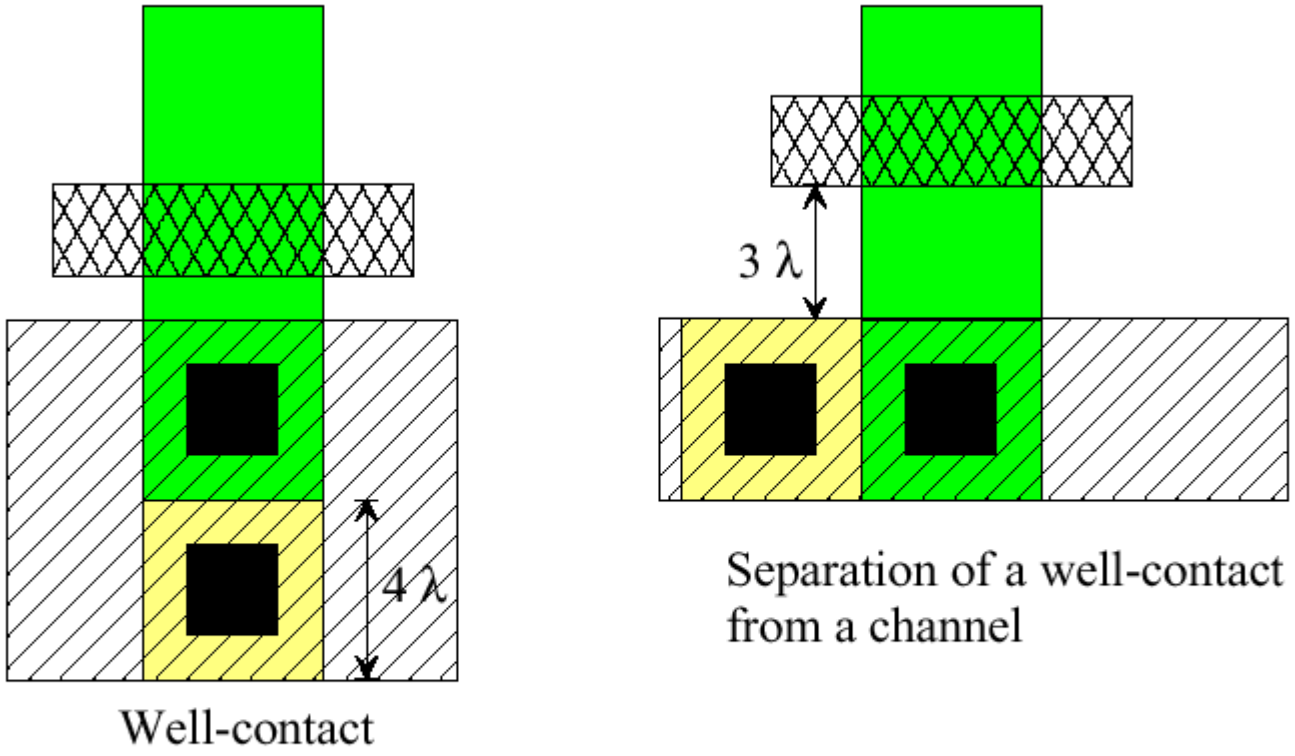


Fig. 3.17 Contact design rules.

Stick Diagram

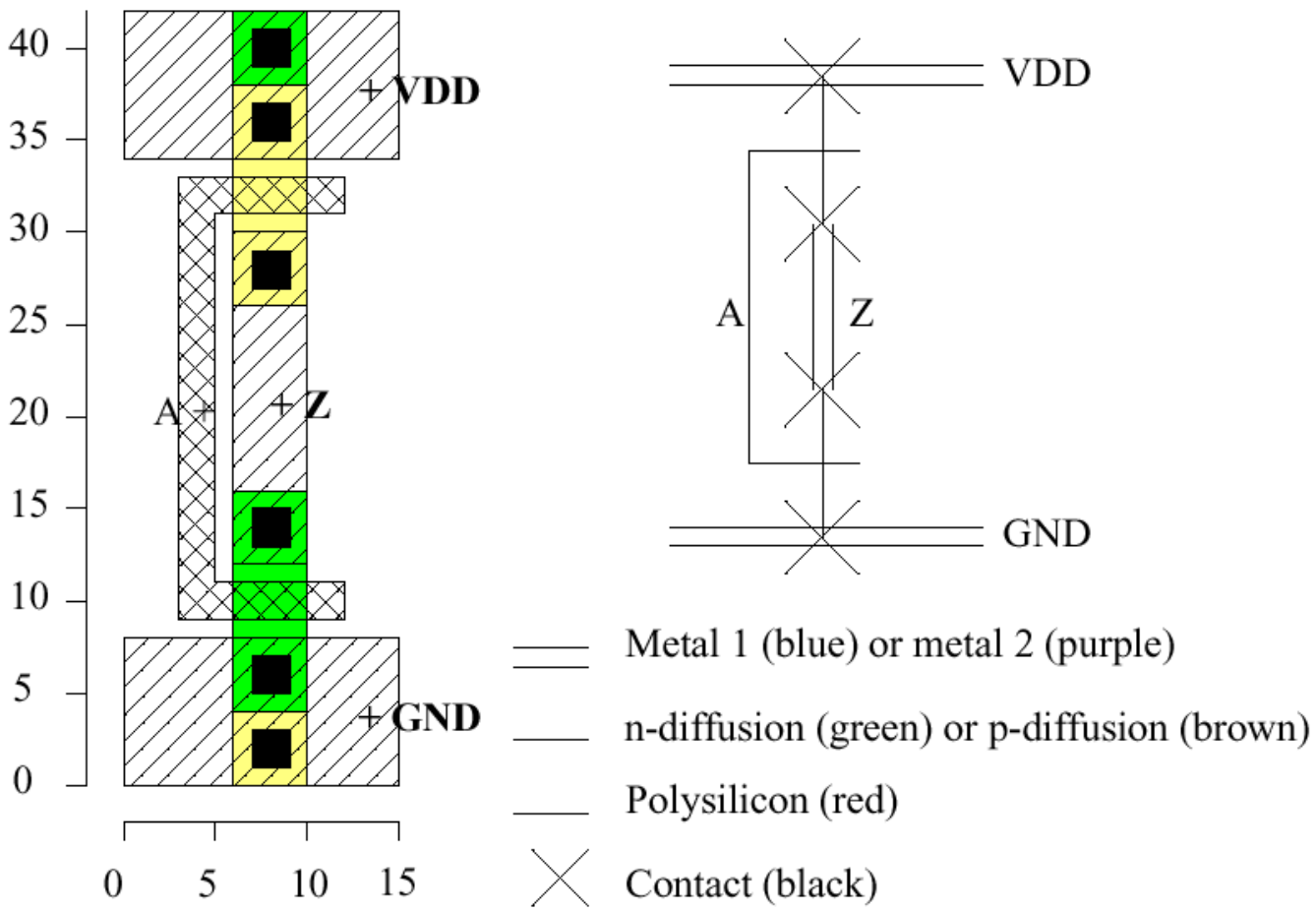


Fig. 3.18 Inverter symbolic layout and its stick diagram.

Inverter Layout

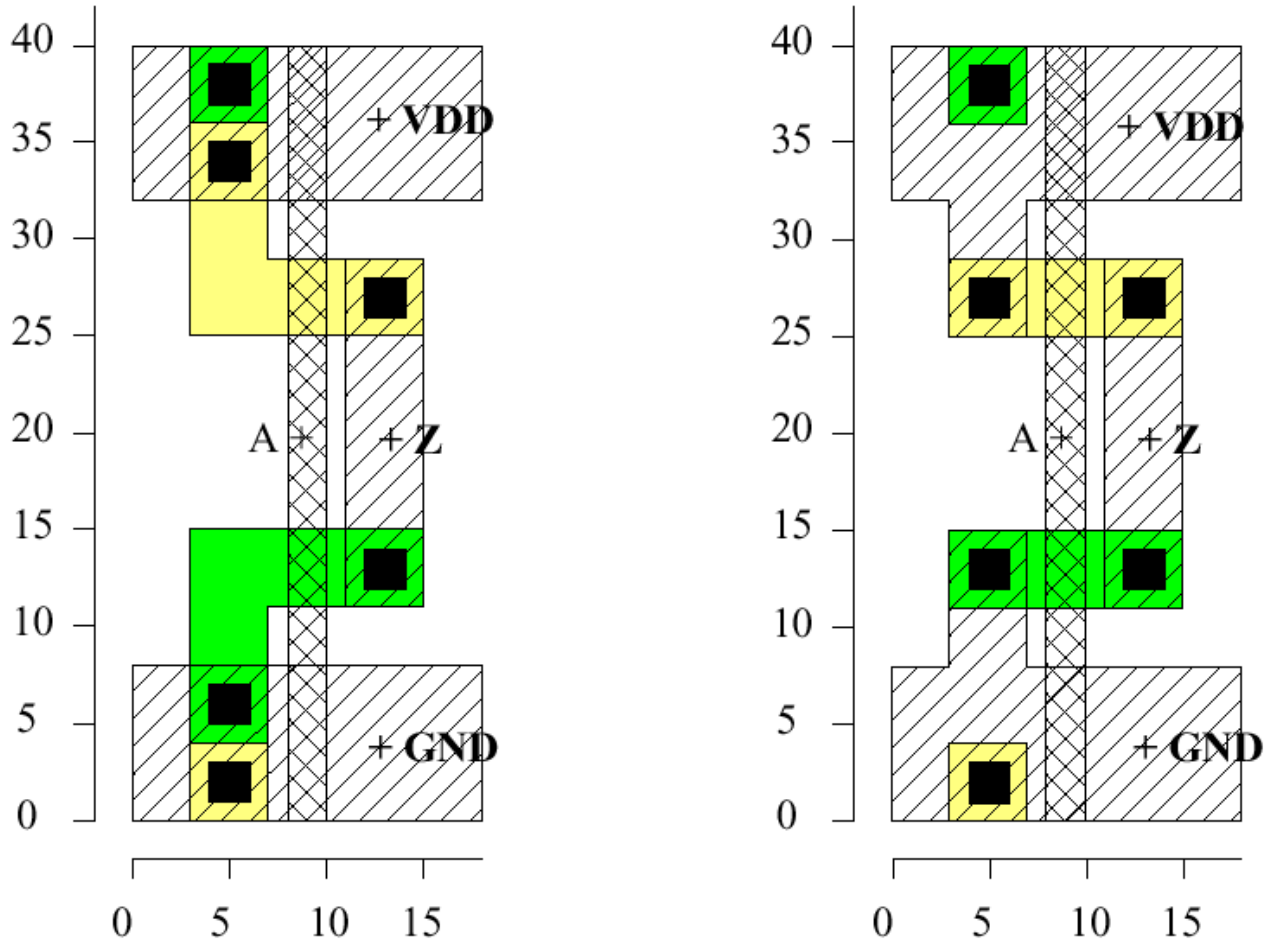


Fig. 3.19 Alternative symbolic layouts for a minimum size inverter.

Inverter Layout

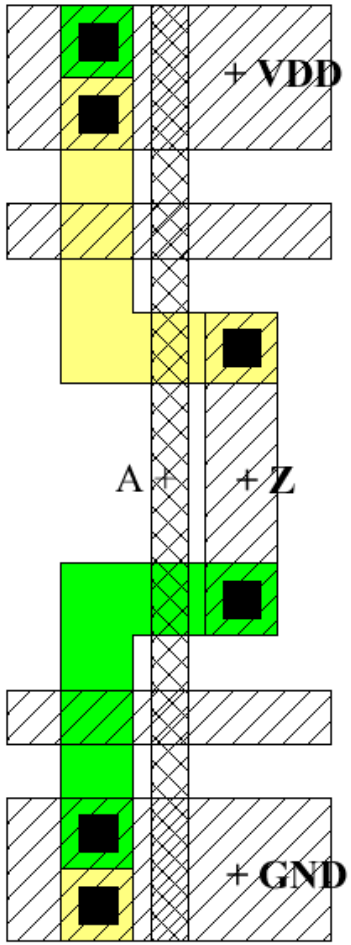


Fig. 3.20 Inverter symbolic layout allowing two horizontal metal-1 routing paths.

Inverter Layout

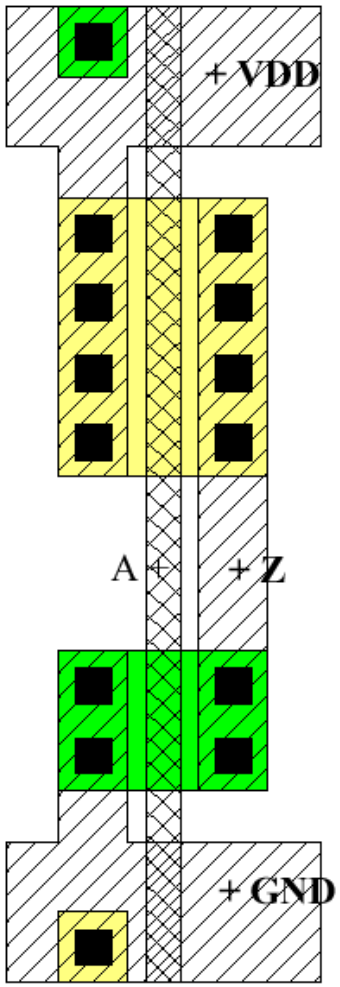


Fig. 3.21 Inverter symbolic layout with wider transistors.

NAND Gate Layout

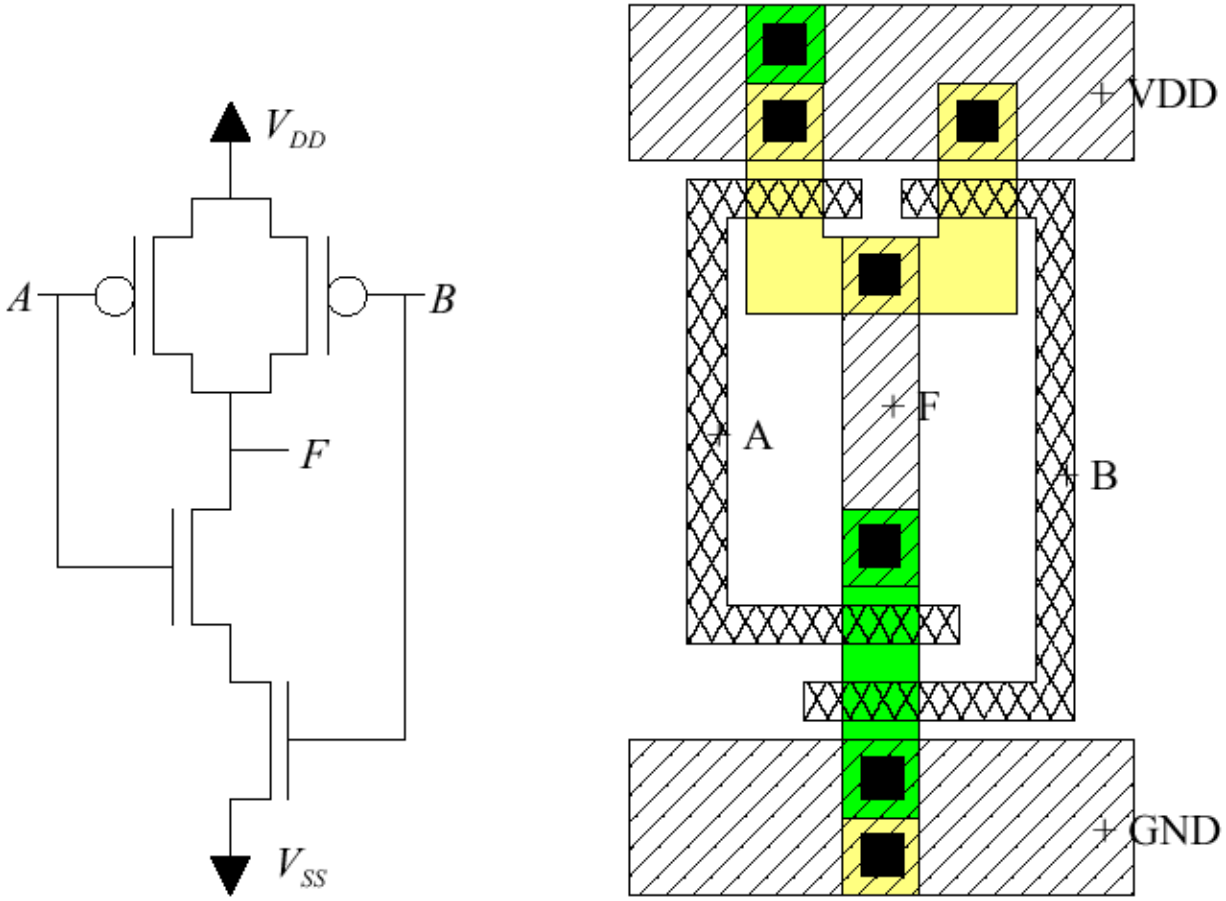


Fig. 3.22 Symbolic layout of a two-input NAND gate.

NAND Gate Layout

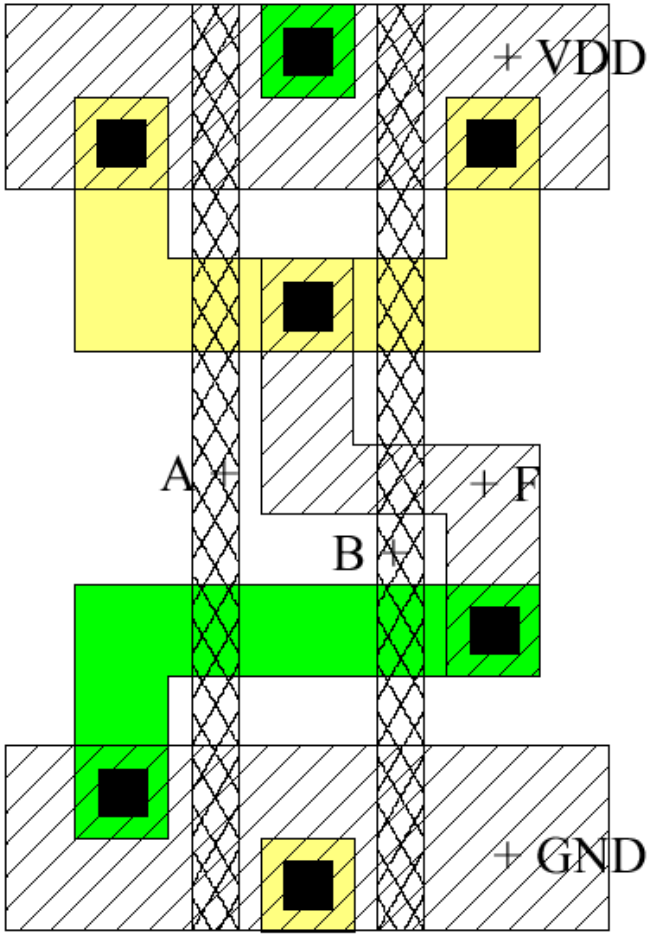


Fig. 3.23 An optimized symbolic layout of a 2-input NAND gate.

Transistor Arrangement

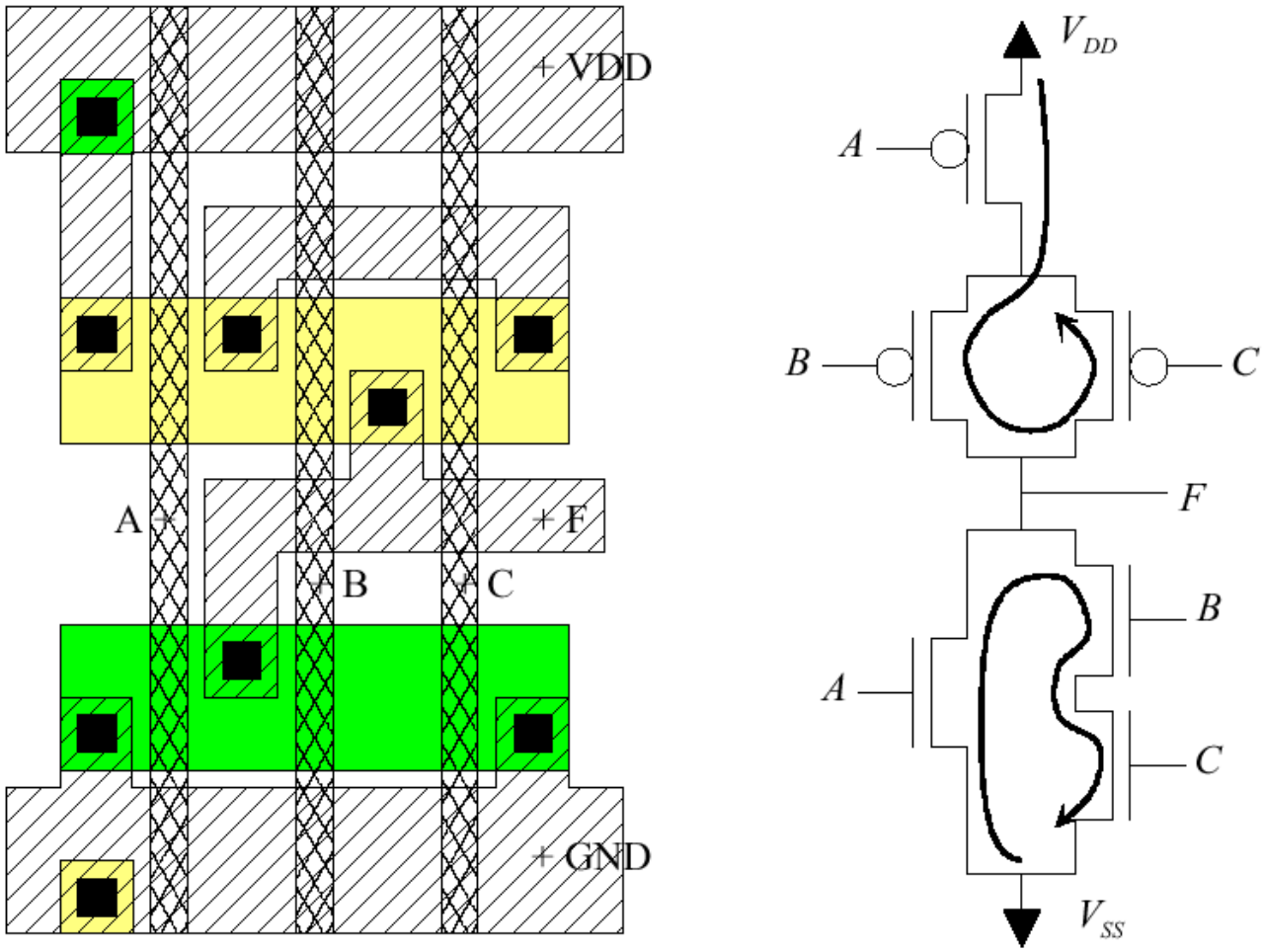


Fig. 3.24 A symbolic layout of $F = \overline{A + BC}$.

Transistor Arrangement

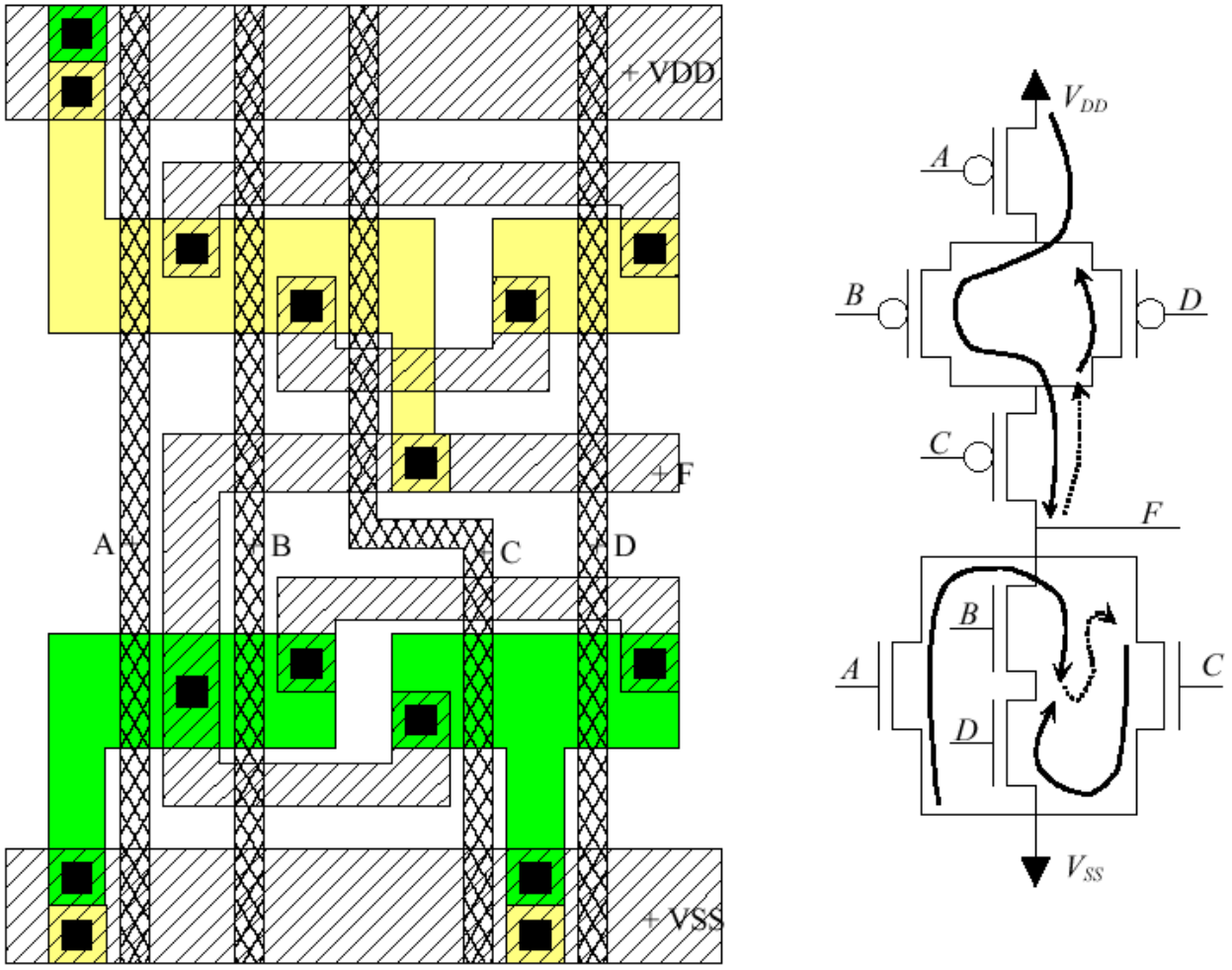


Fig. 3.25 A symbolic layout of $F = \overline{A + BD + C}$.

Standard-Cell Layout

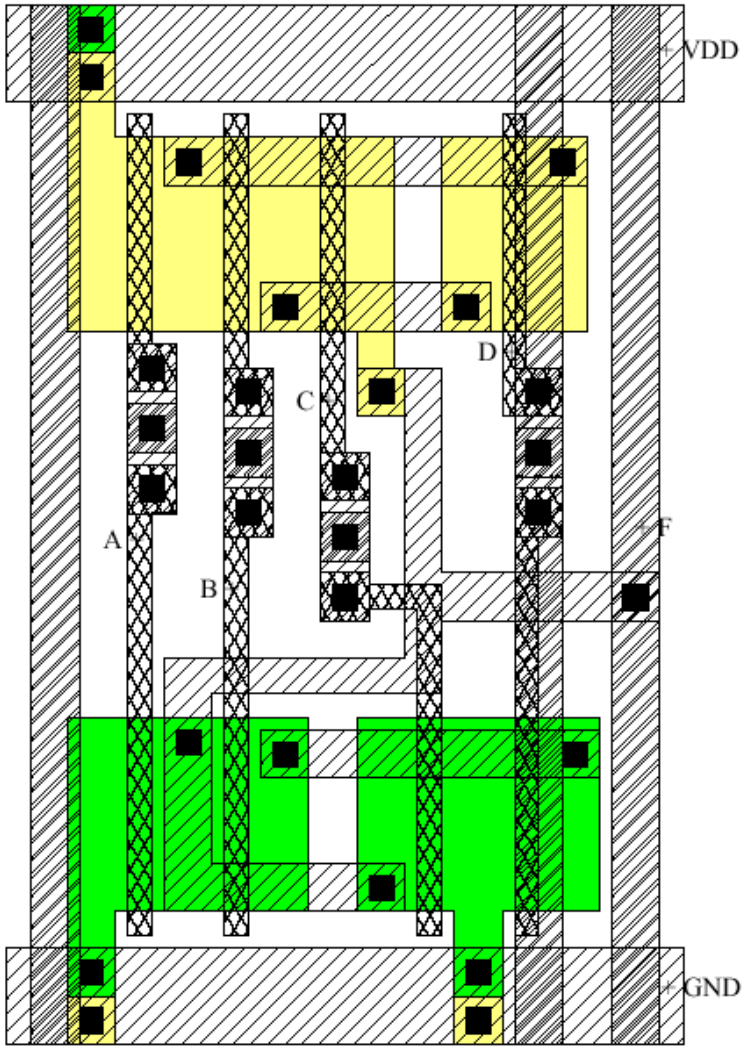


Fig. 3.26 Standard-cell design of $F = \overline{A + BD + C}$.

Standard-Cell Layout

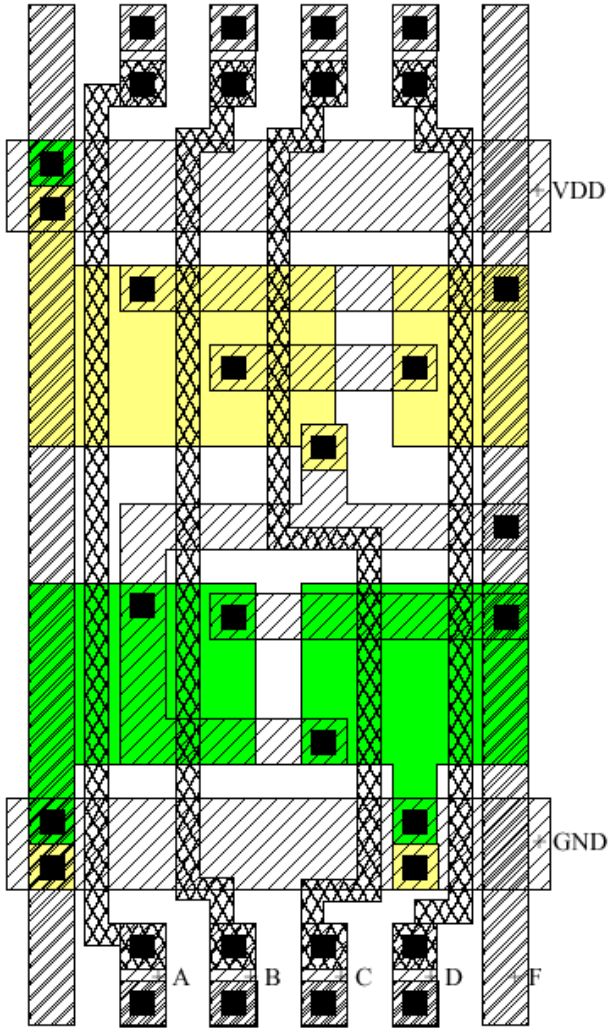


Fig. 3.27 Alternative standard-cell layout of $F = \overline{A + BD + C}$.

Problem 3.3

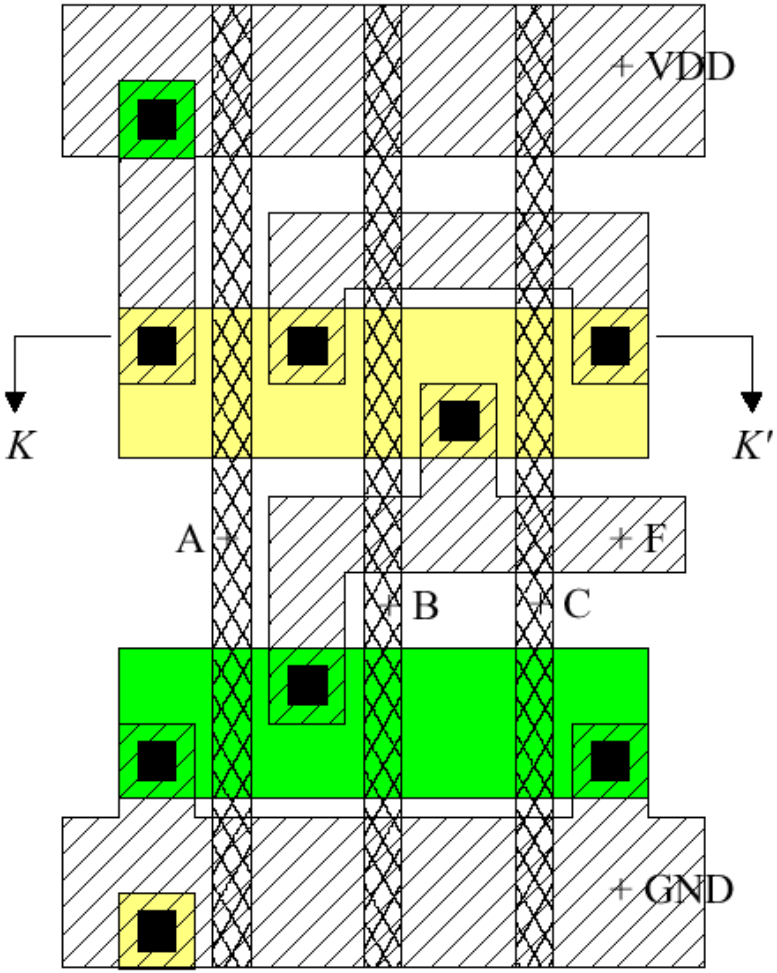


Fig. 3.28 Layout for Problem 3.3.

Problem 3.4

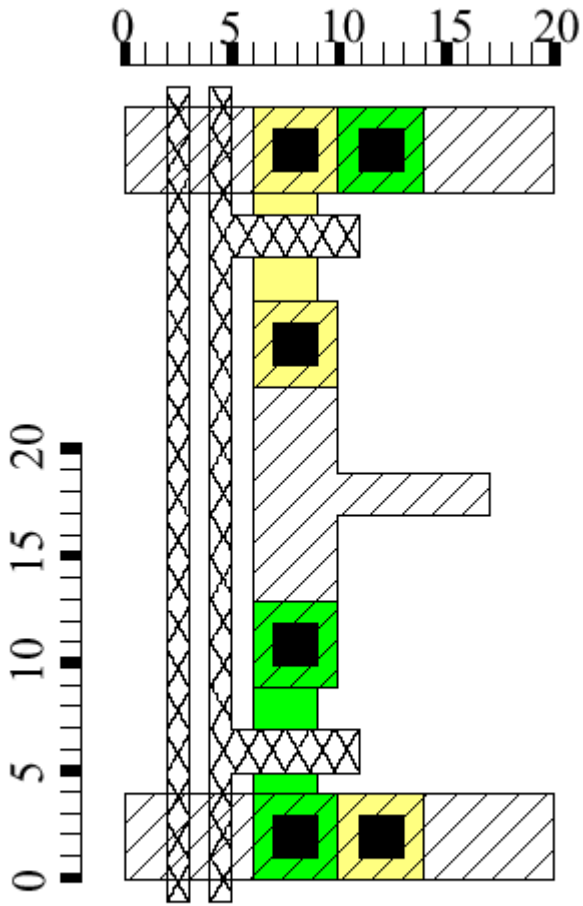


Fig. 3.29 Layout for Problem 3.4.

Problem 3.5

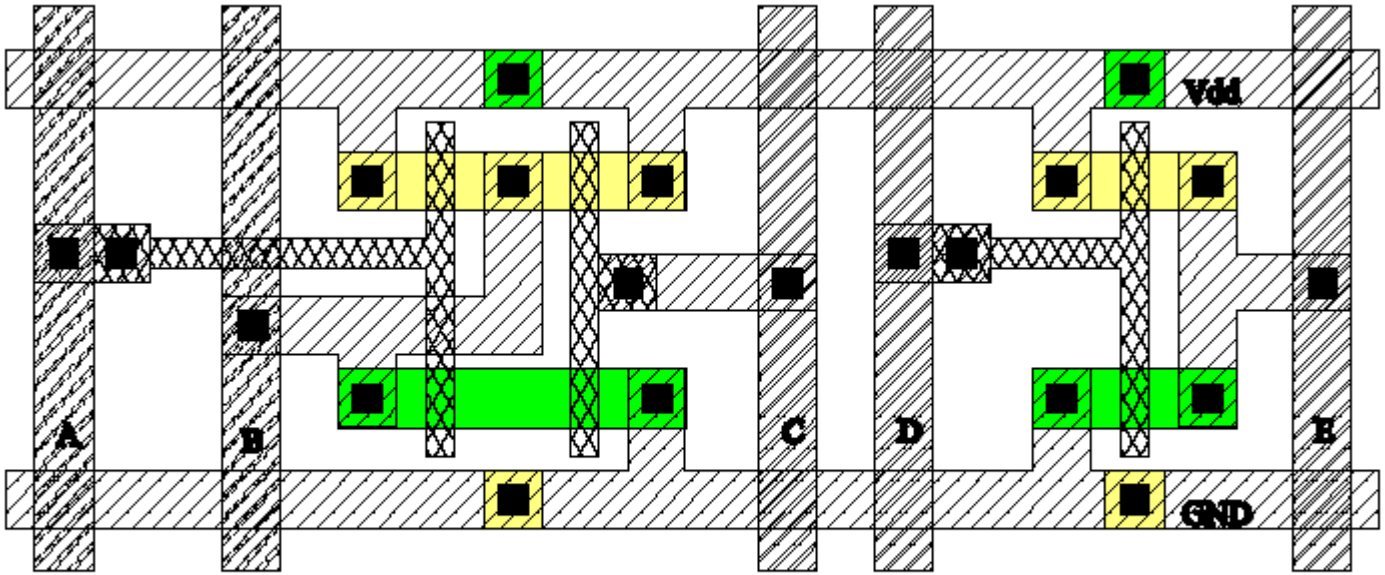


Fig. 3.30 Layout for Problem 3.5.