Chapter 6

Alternative Logic Structures

T-Gate Resistance

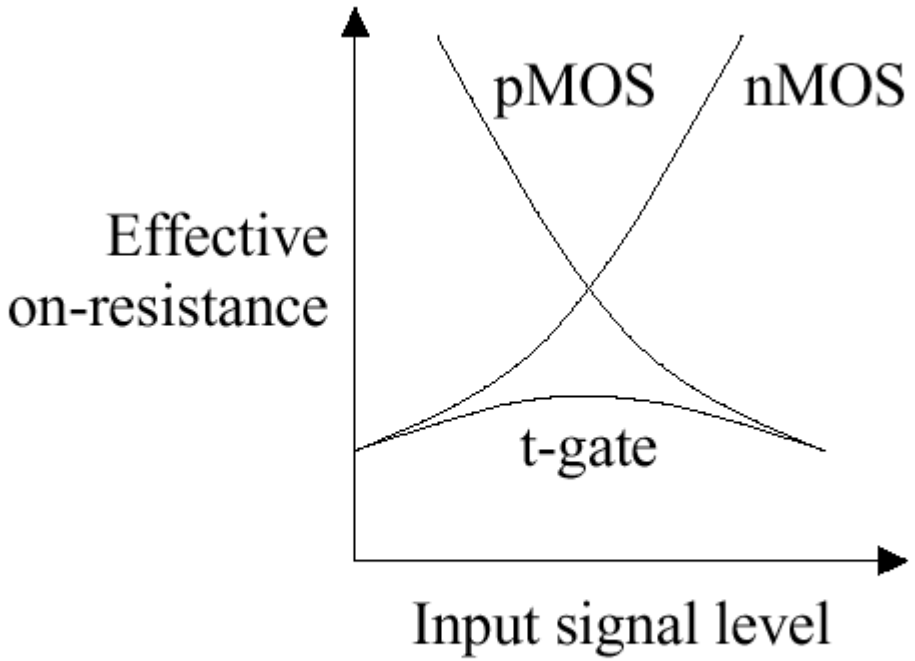

Fig. 6.1 Effective on-resistance of a t-gate.

Open-Drain Inverter

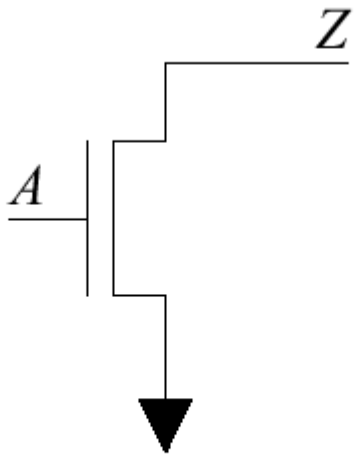

Fig. 6.2 An open-drain inverter.

Open-Drain Inverter

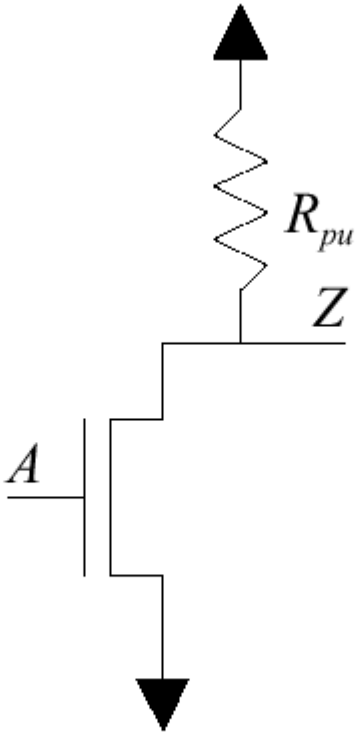

Fig. 6.3 Open drain inverter with a pull-up resistor.

Open-Drain Inverter

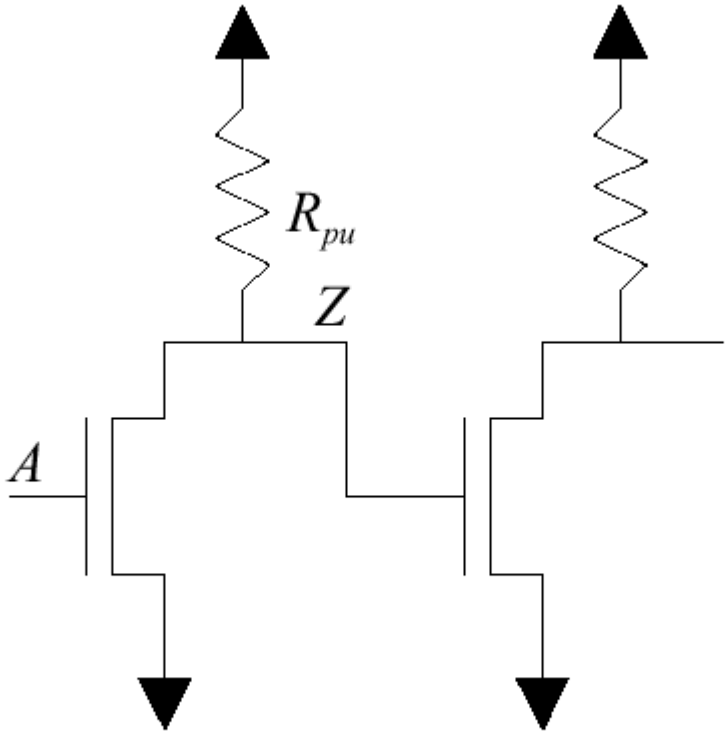

Fig. 6.4 Open-drain inverter driving another open-drain gate.

Pseudo-NMOS Inverter

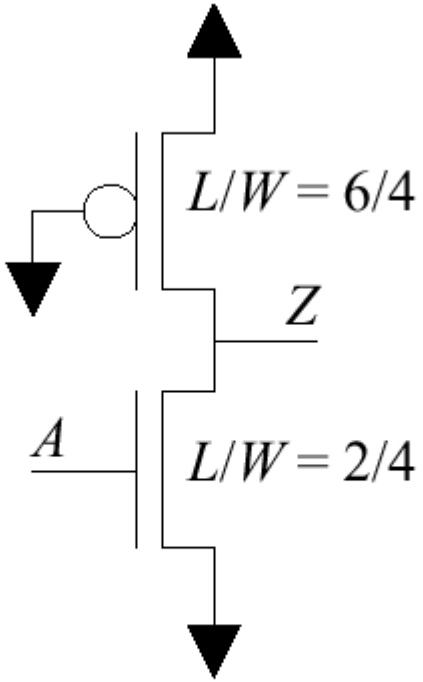

Fig. 6.5 Pseudo-nMOS inverter.

Pseudo-NMOD NAND

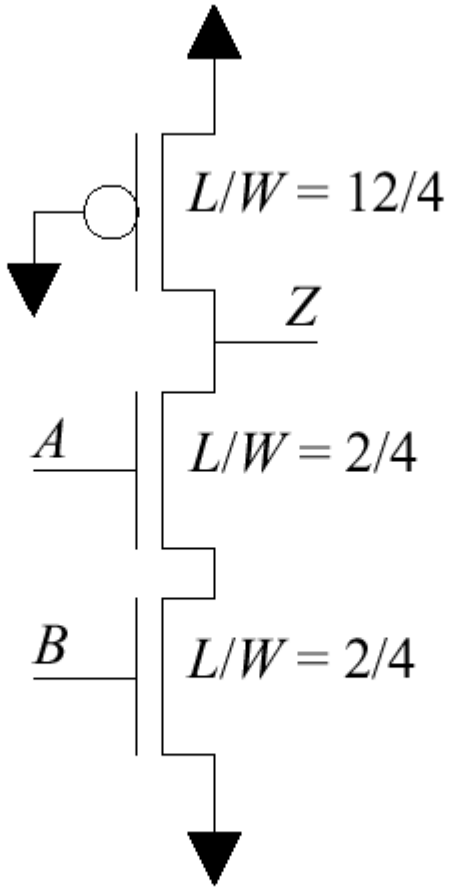

Fig. 6.6 Transistor dimensions of pseudo-nMOS NAND gate.

Pseudo-NMOS NOR

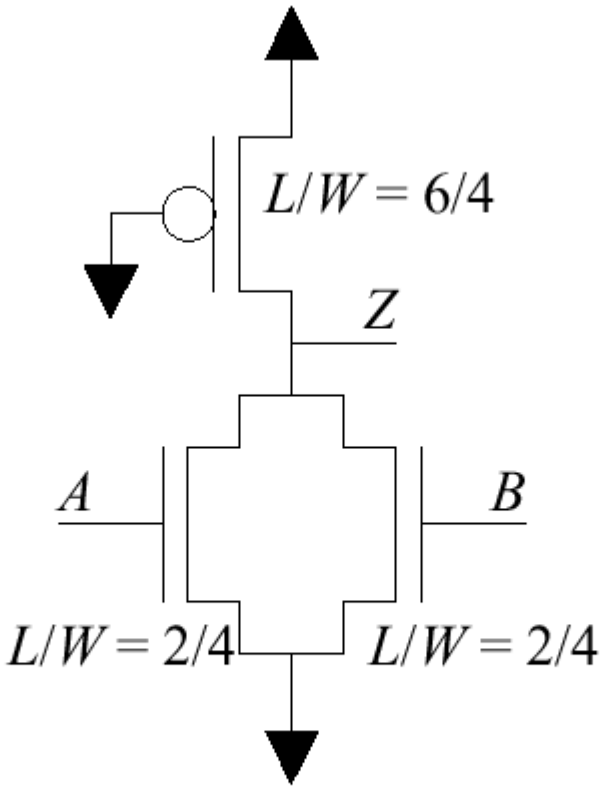

Fig. 6.7 Transistor dimensions of pseudo-nMOS NOR gate.

Pseudo NMOS

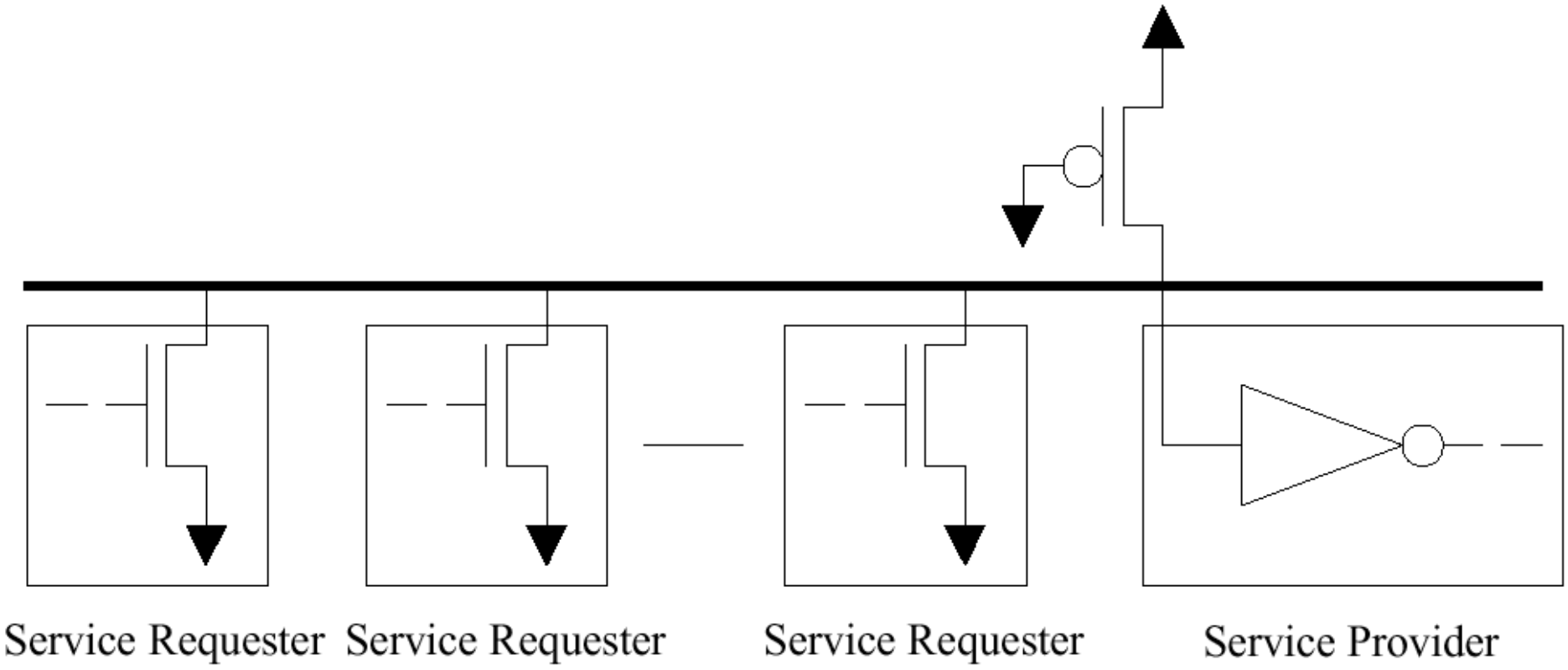

Fig. 6.8 Request line connecting multiple service requesters and a service provider.

PLA

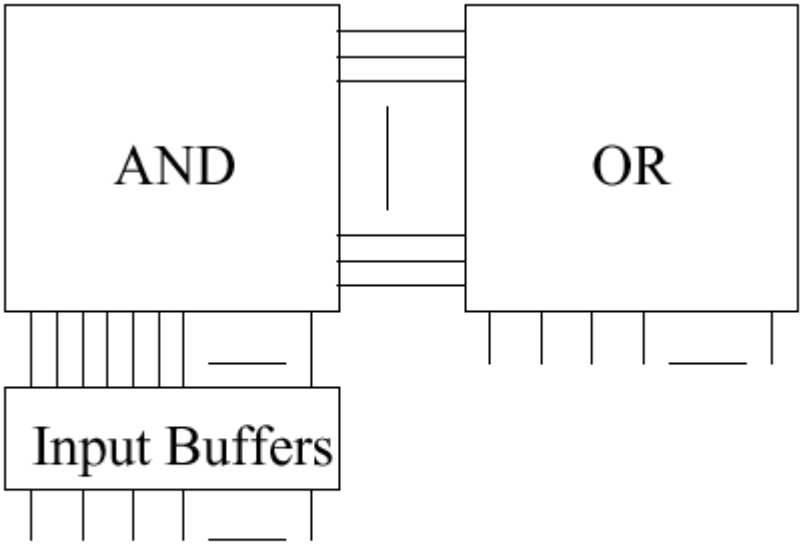

Fig. 6.9 Block diagram of a PLA.

PLA

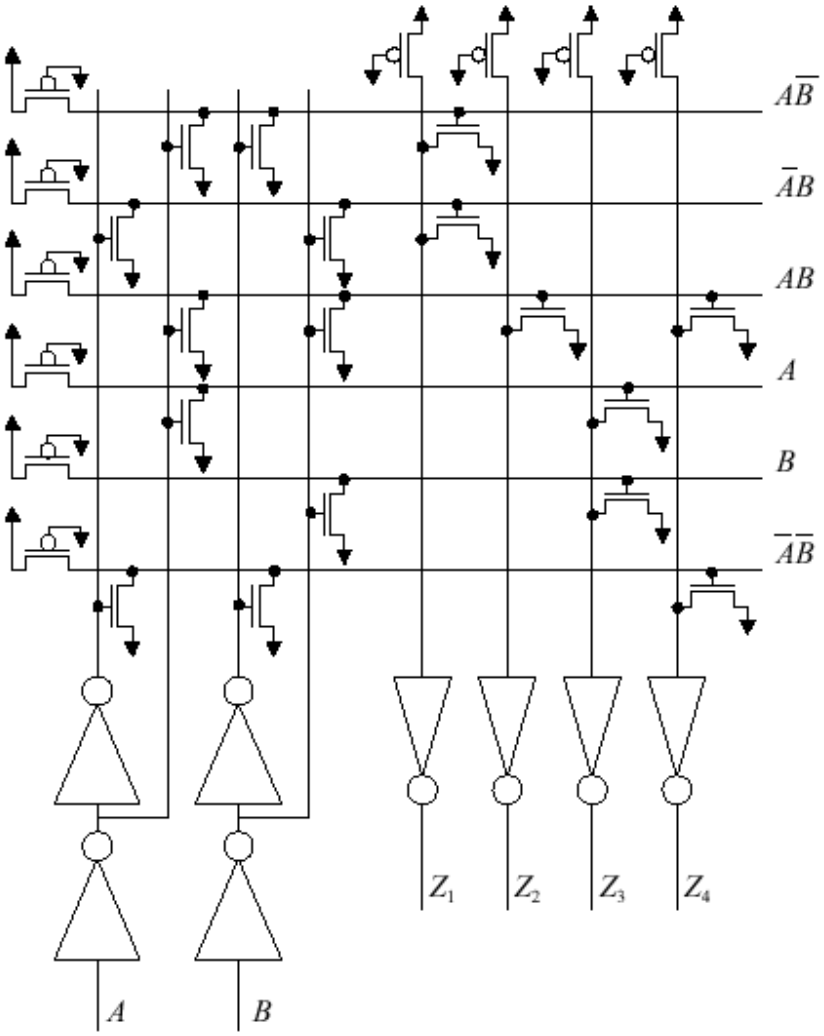

Fig. 6.10 PLA implementation of Example 6.1.

Dynamic CMOS

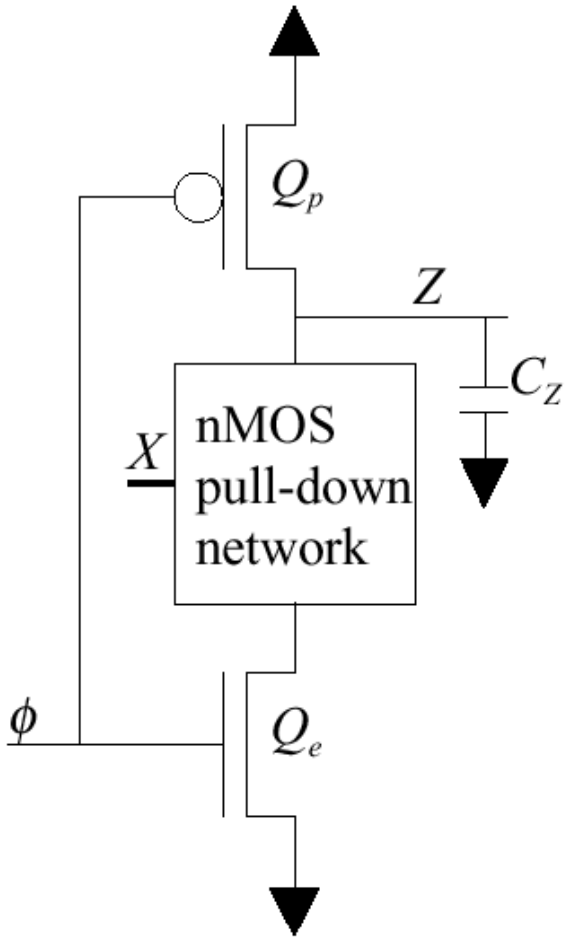

Fig. 6.11 Basic dynamic CMOS logic circuit structure.

Dynamic NAND Gate

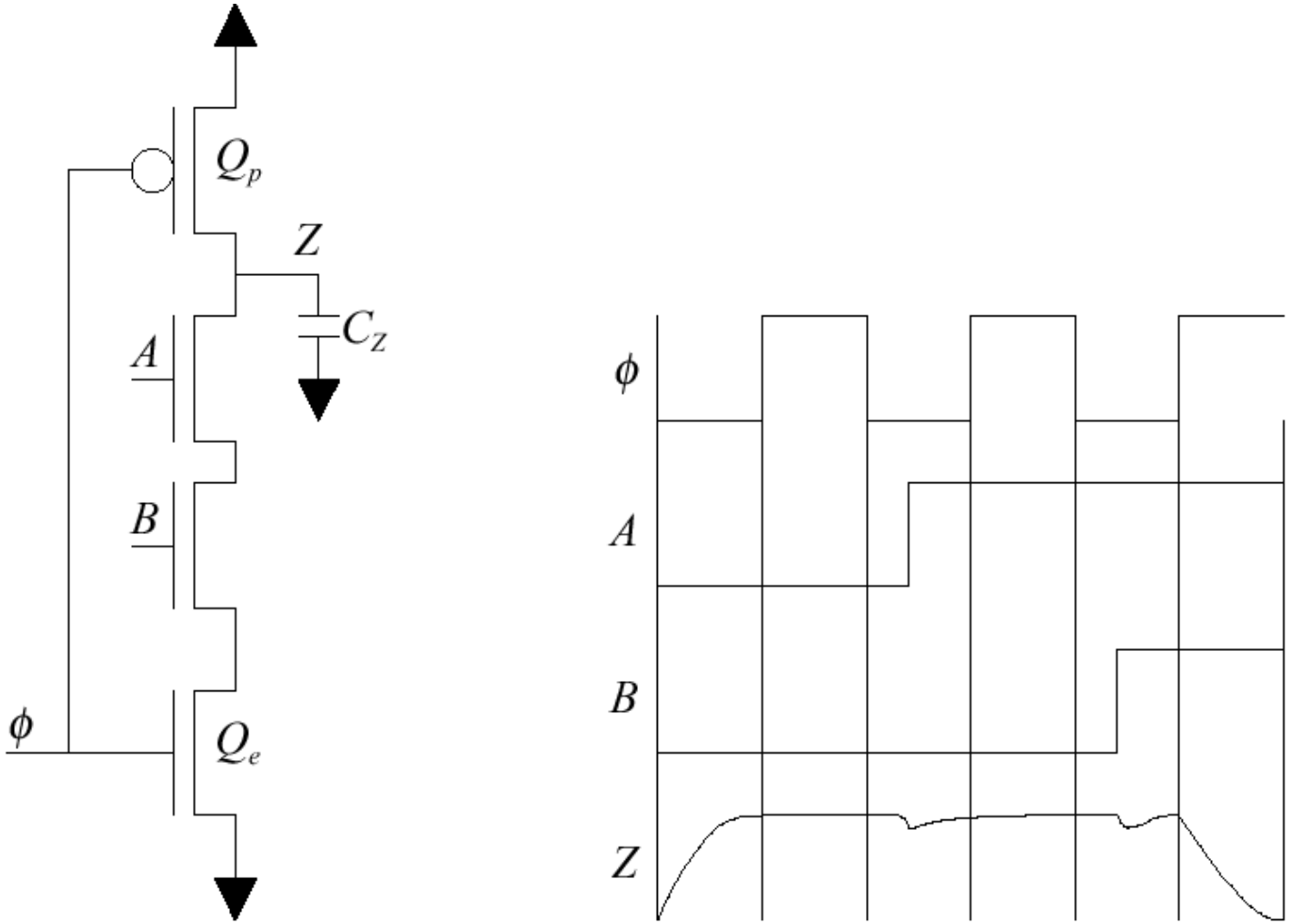

Fig. 6.12 Waveform diagram of a dynamic 2-input NAND gate.

Charge Sharing

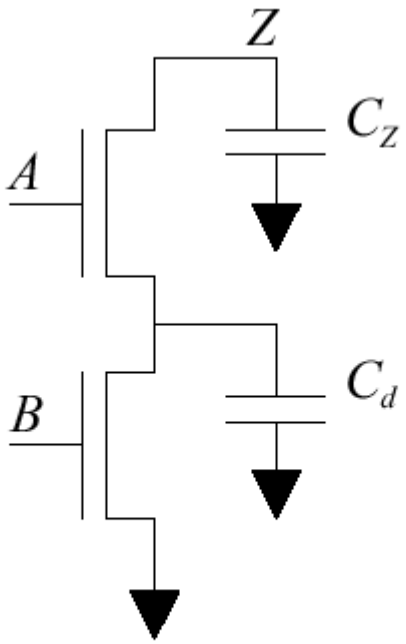

Fig. 6.13 Circuit illustrating charge sharing.

Cascading Dynamic Inverters

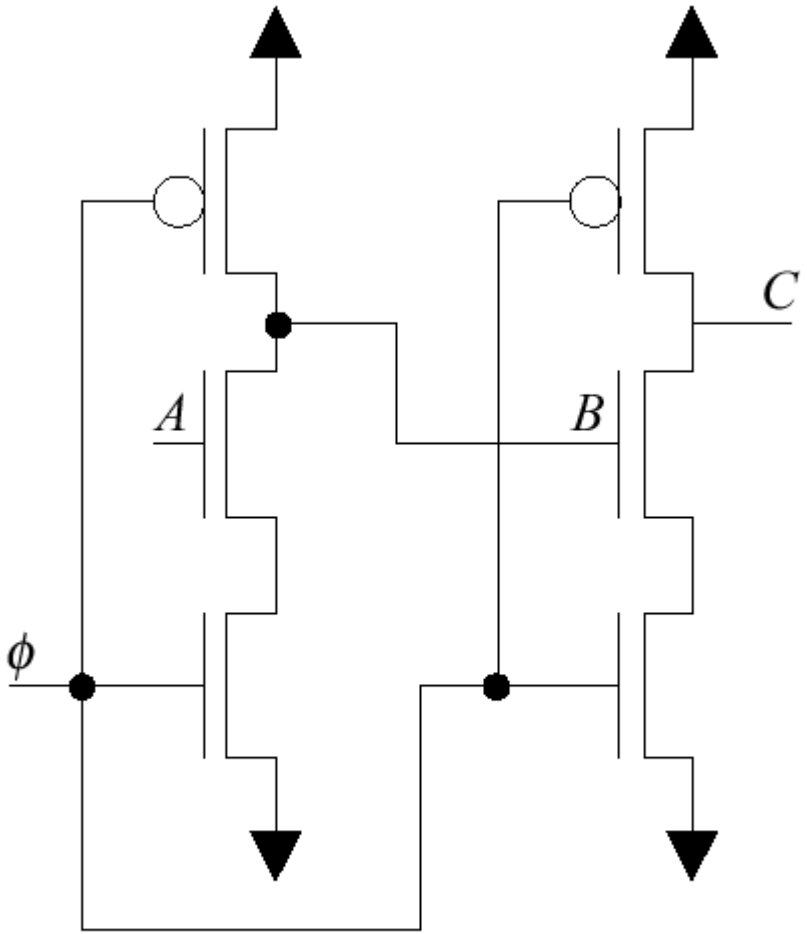

Fig. 6.14 Cascaded dynamic inverters.

Cascading Dynamic Inverters

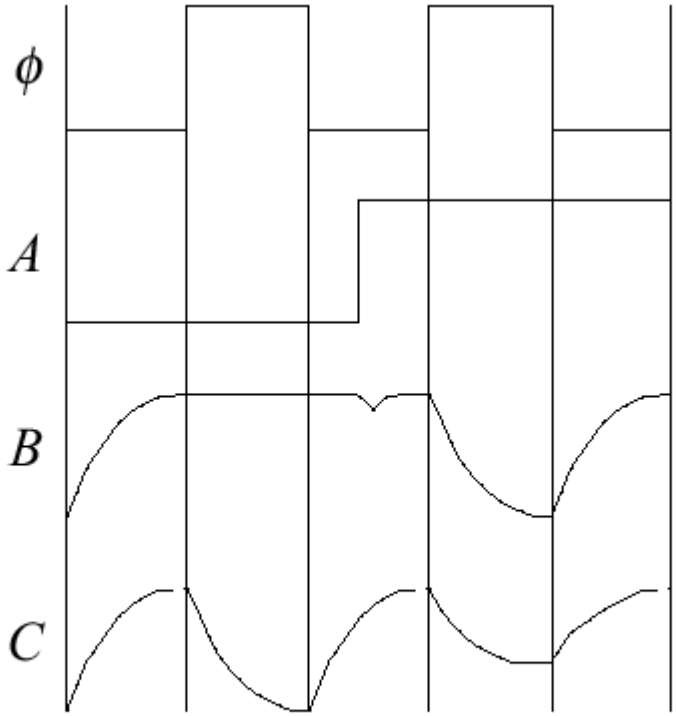

Fig. 6.15 Waveform of two cascading dynamic inverters.

Non-Inverting Domino Logic

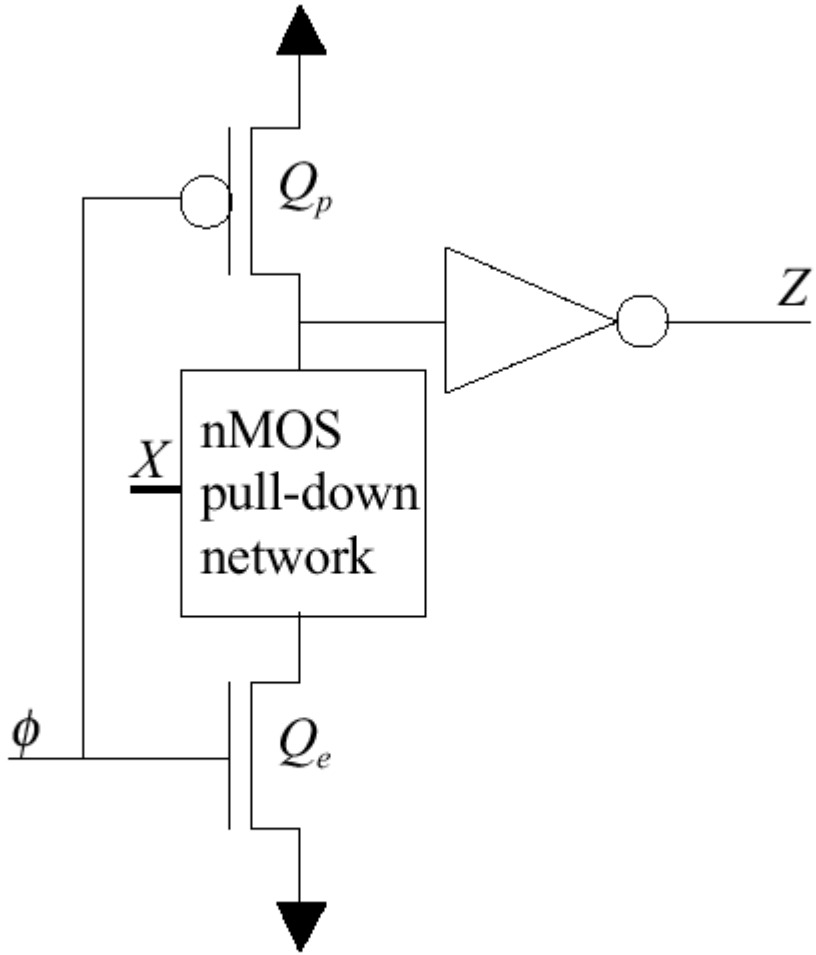

Fig. 6.16 Non-inverting domino logic circuit.

Inverting Domino Logic

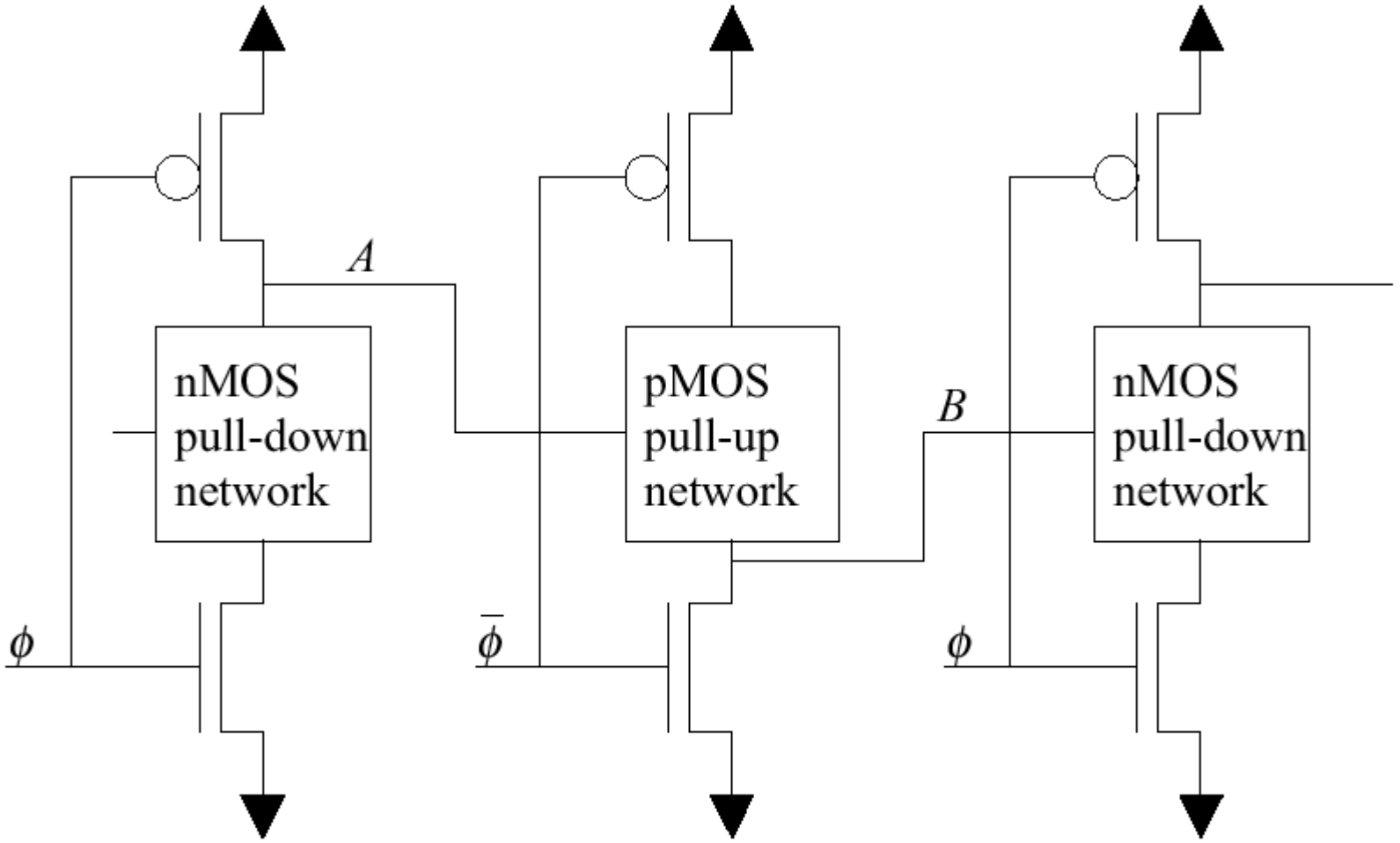

Fig. 6.17 Inverting domino logic circuits.

Dynamic Latch

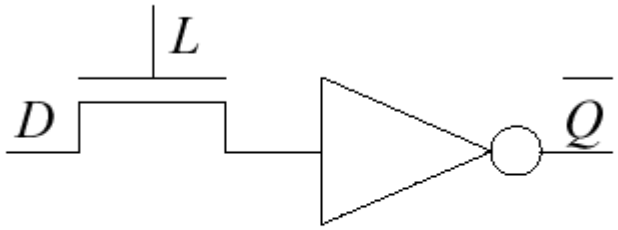

Fig. 6.18 Dynamic D-latch.

Dynamic FF

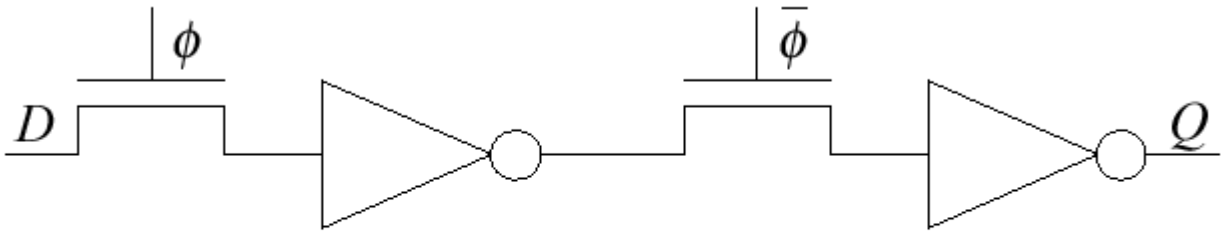

Fig. 6.19 Negative edge triggered D-flip-flop.

BICMOS Inverter

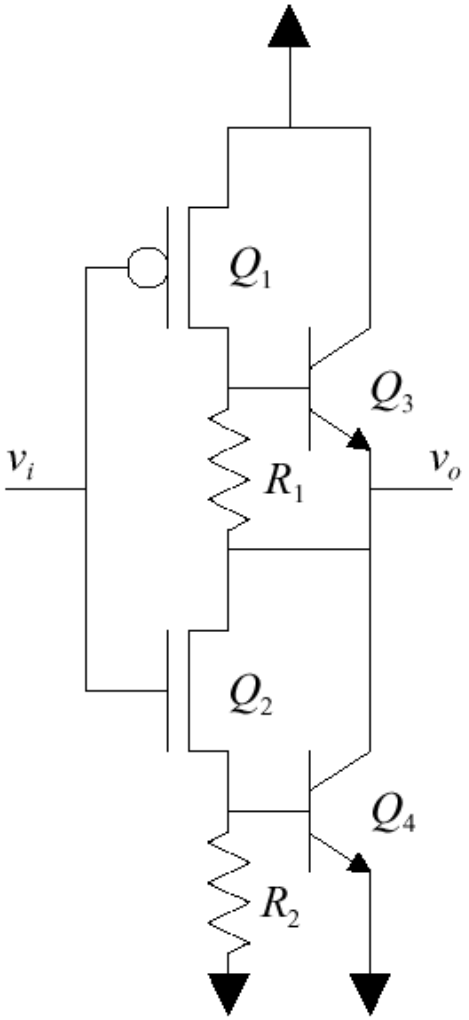

Fig. 6.20 BiCMOS inverter.

BICMOD NAND Gate

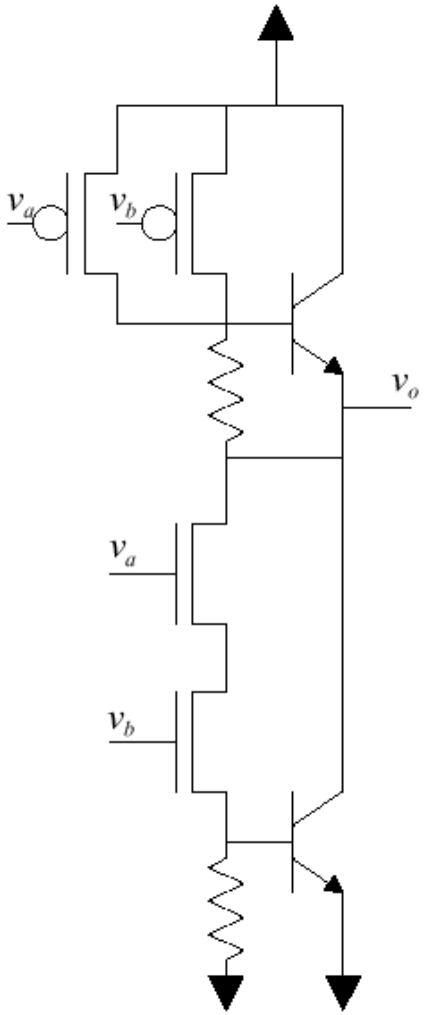

Fig. 6.21 BiCMOS 2-input NAND gate.

Problem 6.6

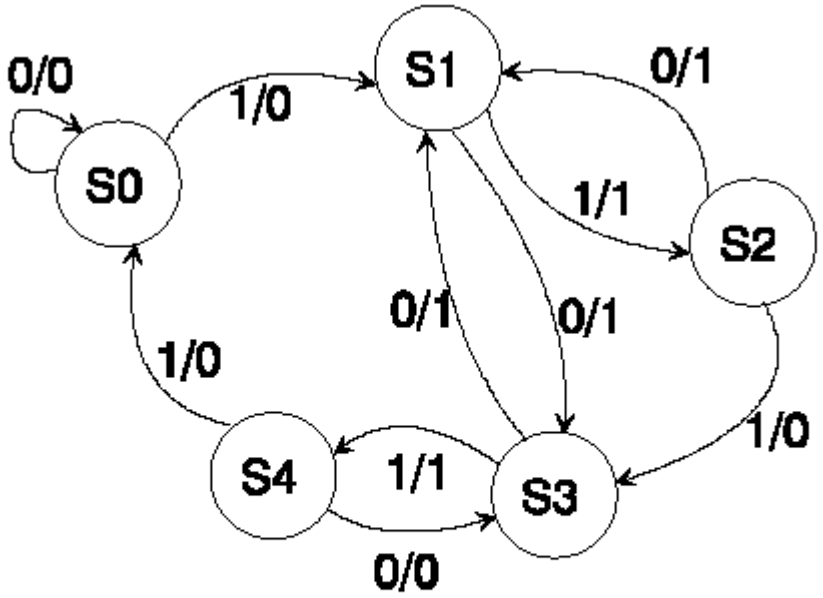

Fig. 6.22 State diagram for problem 6.6.

Problem 6.11

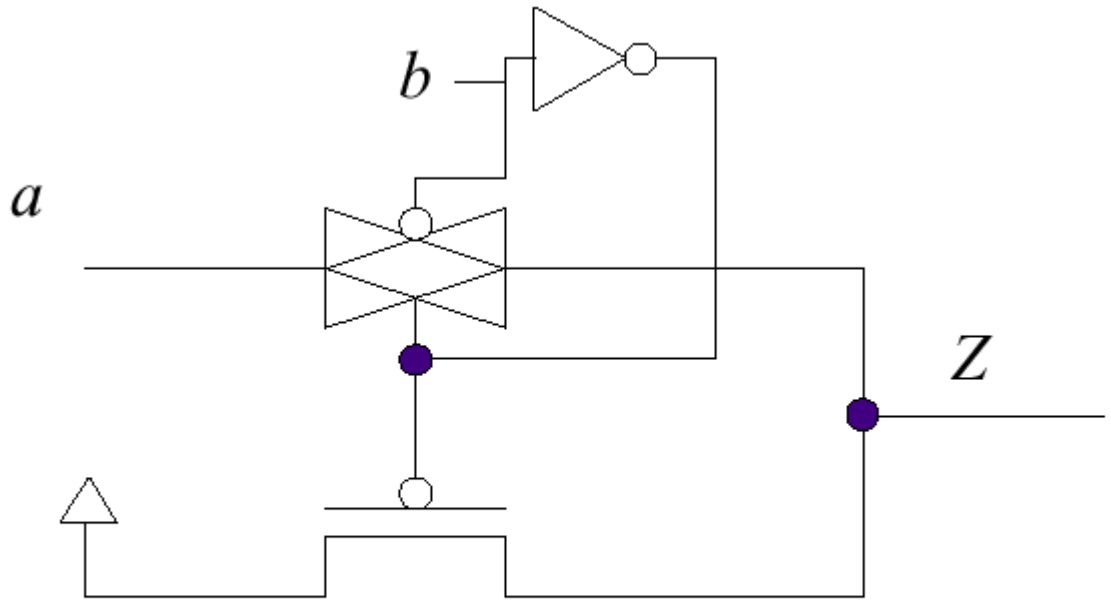

Fig. 6.23 Circuit for Problem 6.11.

Problem 6.12

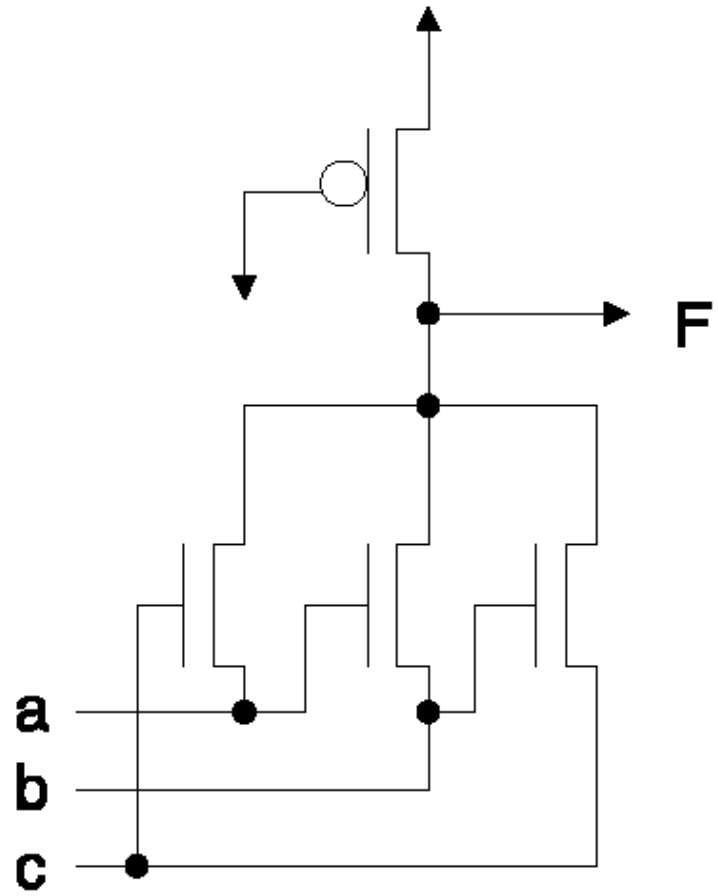

Fig. 6.24 Circuit diagram for Problem 6.12.