Chapter 9

Testing

Fault Examples

Design errors	Incomplete specifications
	Incorrect logic implementations
	Incorrect wiring
	Design rule violations
	Excessive delays
	Glitches or hazards
	Slow rise/fall times
	Improper noise margins
	Improper timing margins
Fabrication errors	Shorts
	Opens
	Improper doping profiles
	Mask misalignments
	Incorrect transistor threshold voltages
Physical failures	Electron migration
	Cosmic radiation and α-particles

Fig. 9.1 Example faults found in integrated circuits.

NAND Gate

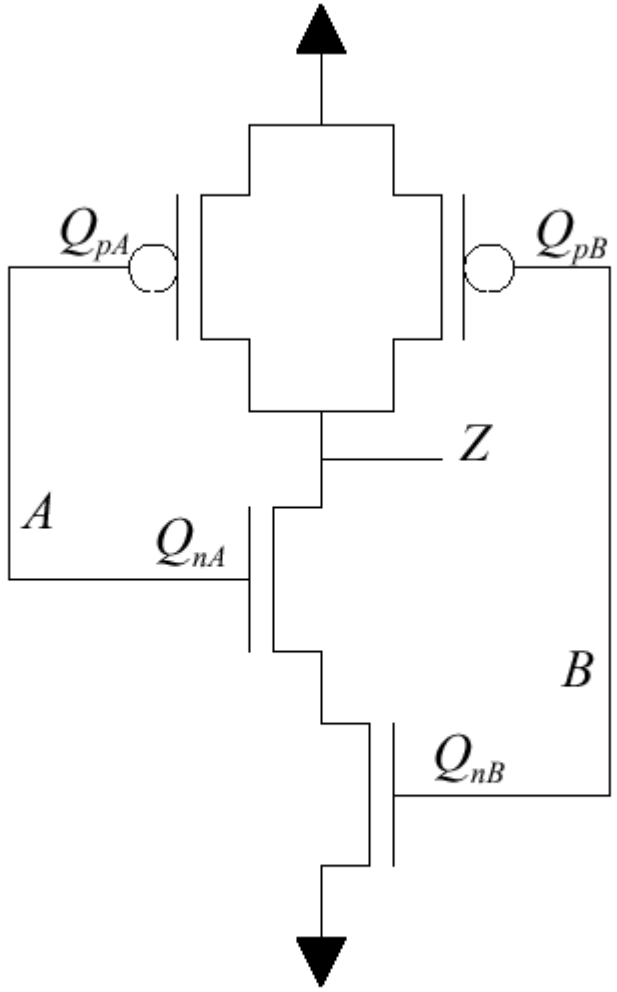


Fig. 9.2 CMOS NAND gate.

Example Circuit

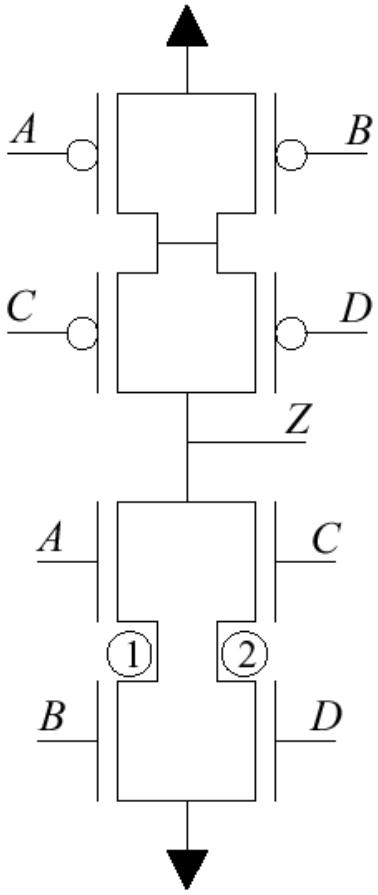


Fig. 9.3 CMOS implementation of $Z = \overline{AB + CD}$.

NAND Gate Possible Faults

AB	Z (fault-free)	Z (A: s-a-1)	Z (A: s-a-0)	Z (Q_{nA}: s-op)	Z (Q_{nA}: bridged)
00	1	1	1	1	1
01	1	0	1	1	X
10	1	1	1	1	1
11	0	0	1	HiZ	0

Fig. 9.4 A few possible faults in a CMOS NAND gate.

D-Algorithm

AND	0	1	D	$\bar{D}$	X
0	0	0	0	0	0
1	0	1	D	$\bar{D}$	X
D	0	D	D	0	X
$\bar{D}$	0	$\bar{D}$	0	$\bar{D}$	X
X	0	X	X	X	X

OR	0	1	D	$\bar{D}$	X
0	0	1	D	$\bar{D}$	X
1	1	1	1	1	1
D	D	1	D	1	X
$\bar{D}$	$\bar{D}$	1	1	$\bar{D}$	X
X	X	1	X	X	X

Fig. 9.5 5-valued logic operations in D-algorithm.

NAND Gate

Fig. 9.6 2-input NAND gate.

NAND Truth Table

a	*b*	*c*: s-a-0
X	*X*	0

Fig. 9.7 Truth table of a NAND gate with its output s-a-0.

NAND Gate Singular Cover

a	b	$\overline{ab}$
0	X	1
X	0	1
1	1	0

Fig. 9.8 Singular cover for two-input NAND gate.

Intersecting Rules

Intersect ($\wedge$)	0	1	X
0	0	$\bar{D}$	0
1	D	1	1
X	0	1	X

Fig. 9.9 Intersecting rules.

NOR Gate Singular Cover

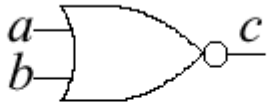


Fig. 9.10 Two-input NOR gate.

a	b	c
0	X	1
1	X	0

Fig. 9.11 Singular cover for NOR gate with b: s-a-0.

NOR Gate Singular Cover

a	b	c
0	0	1
1	X	0
X	1	0

Fig. 9.12 Singular cover for fault-free NOR gate.

D-Algorithm

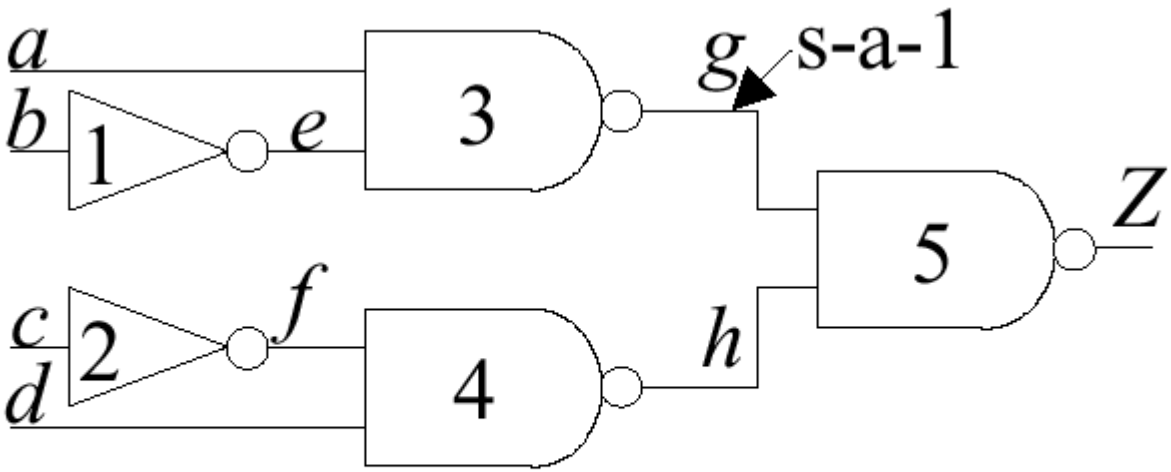


Fig. 9.13 Example circuit for D-algorithm.

D-Algorithm

	a	b	c	d	e	f	g	h	Z
Primitive D-cube (gate 3)	1				1		D		
Propagation D-cube (gate 5)							D	1	$\bar{D}$
Singular cover (gate 1)		0			1				
Singular cover (gate 4)				X		0		1	
Singular cover (gate 2)			1			0			

Fig. 9.14 D-algorithm.

Bridging

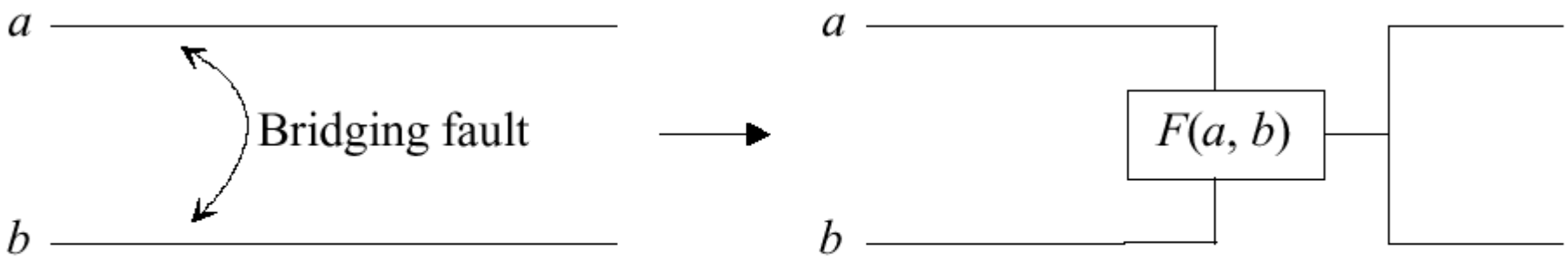


Fig. 9.15 Bridging fault model.

Full Adder

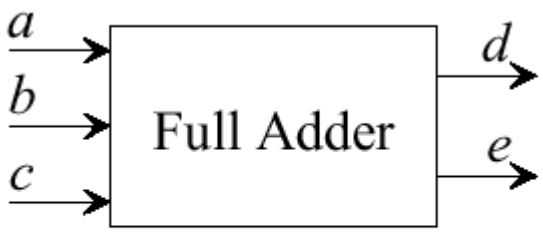


Fig. 9.16 Full adder.

Test Patterns

Fault	Test Patterns (*abc*)	Fault-free output (*de*)	Faulty output (*de*)
a: s-a-1	000	00	01
	001	01	10
	010	01	10
	011	10	11
b: s-a-1	000	00	01
	001	01	10
	100	01	10
	101	10	11
c: s-a-1	000	00	01
	010	01	10
	100	01	10
	110	10	11
a: s-a-0	111	11	10
	100	01	00
	101	10	01
	110	10	01
b: s-a-0	111	11	10
	010	01	00
	011	10	01
	110	10	01
c: s-a-0	111	11	10
	001	01	00
	011	10	01
	101	10	01
d: s-a-1	000	00	10
	001	01	11
	010	01	11
	100	01	11
e: s-a-1	110	10	11
	000	00	01
d: s-a-0	011	10	00
	101	10	00
	110	10	00
	111	11	01
e: s-a-0	001	01	00
	010	01	00
	100	01	00
	111	11	10

Fig. 9.17 Test patterns for all stuck-at faults in a full adder.

Fault Matrix

Test vector	a s-a-1	b s-a-1	c s-a-1	a s-a-0	b s-a-0	c s-a-0	d s-a-1	e s-a-1	d s-a-0	e s-a-0
000	1	1	1				1	1		
001	1	1				1		1	1	
010	1		1		1			1	1	
011	1				1	1				
100		1	1	1				1	1	
101		1		1		1				1
110			1	1	1		1			1
111				1	1	1			1	1

Fig. 9.18 Fault matrix.

Full Adder Implementation

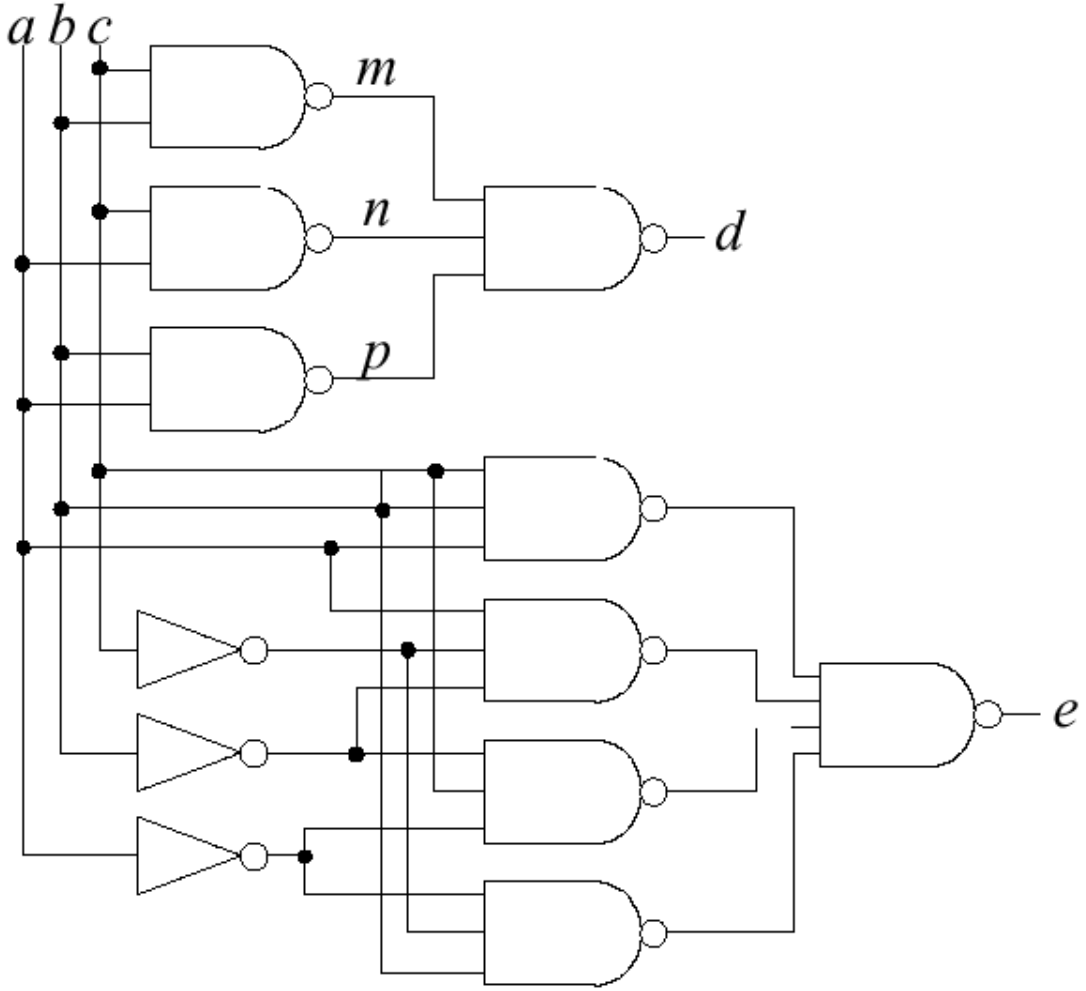


Fig. 9.19 A gate level implementation of a full adder.

Sequential Circuit Testing

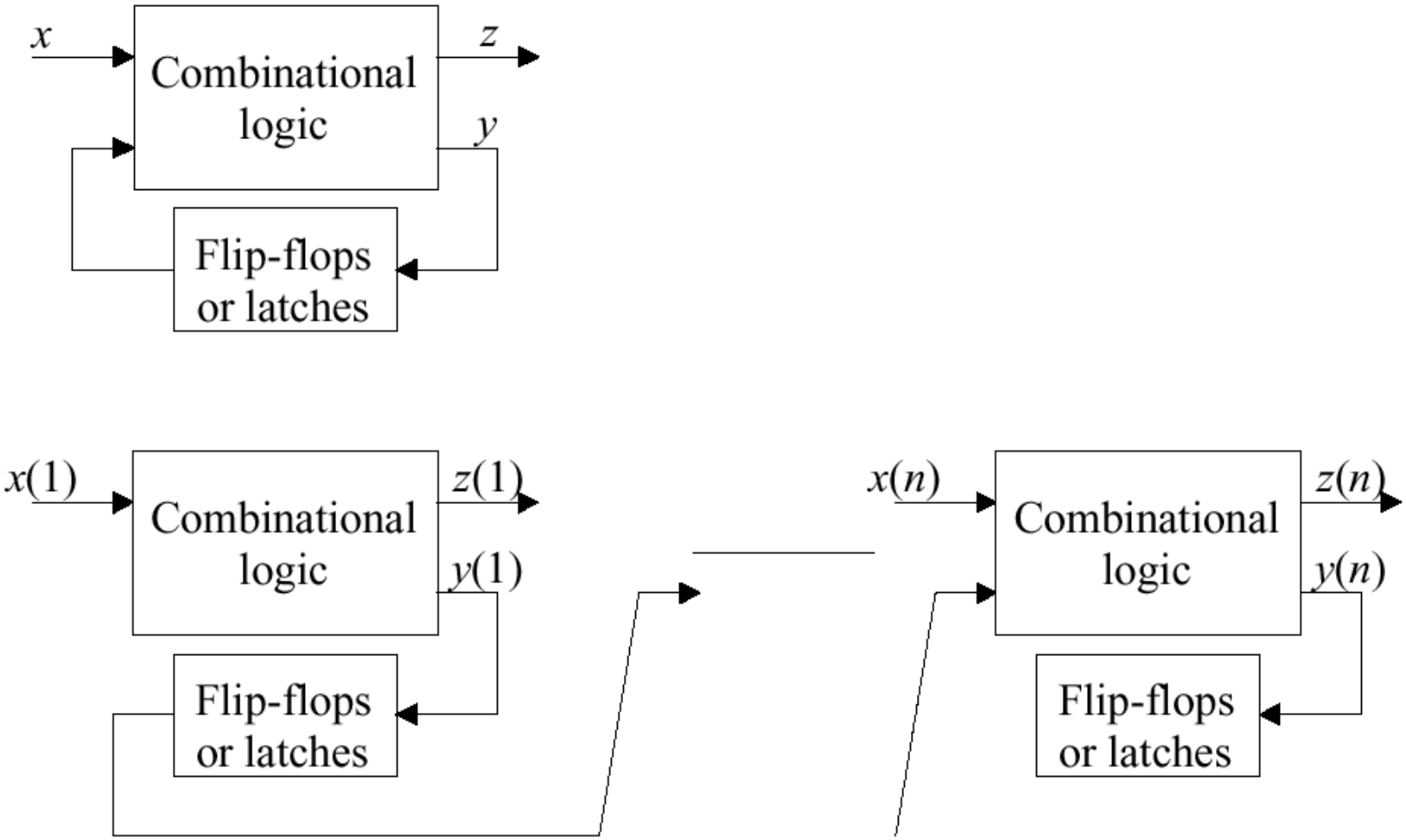
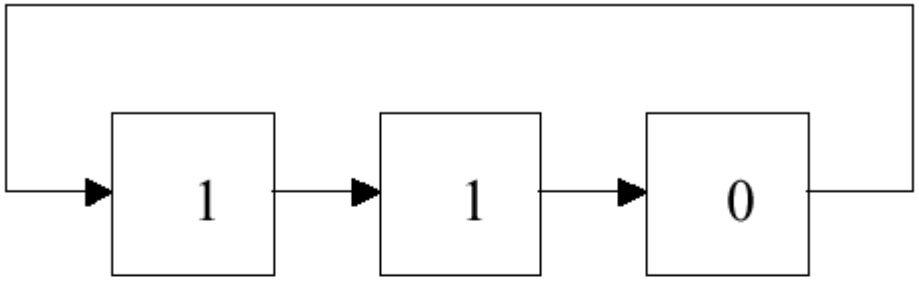


Fig. 9.20 Sequential circuit modeled as combinational circuit for test generation.

Shift Register with Feedback



0	1	1
1	0	1
1	1	0

Fig. 9.21 Shift register with feedback.

Linear Feedback Shift Register

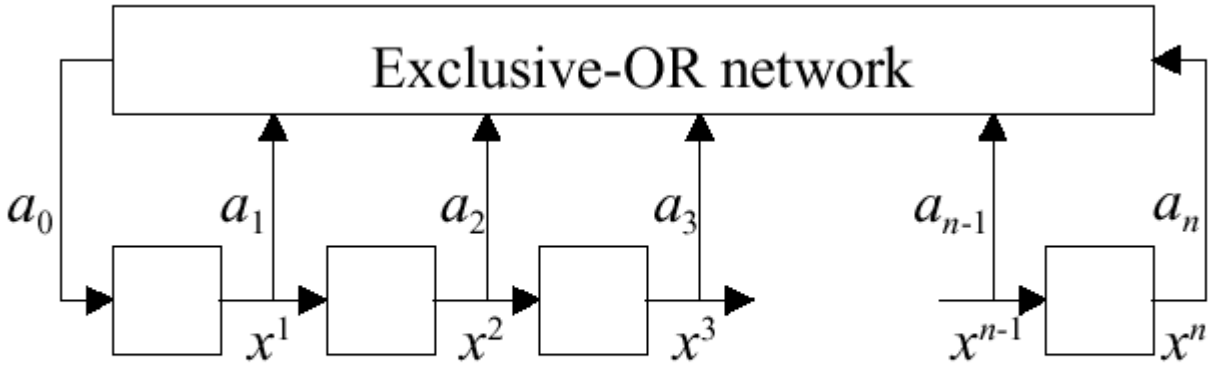
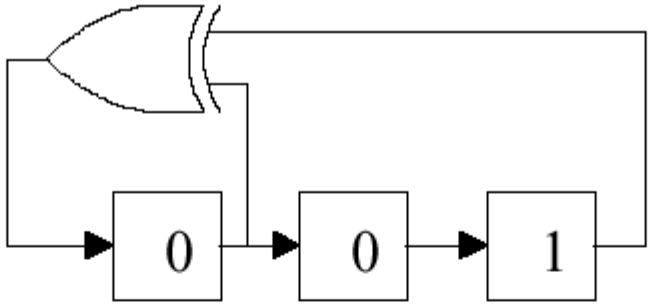


Fig. 9.22 Linear feedback shift register.

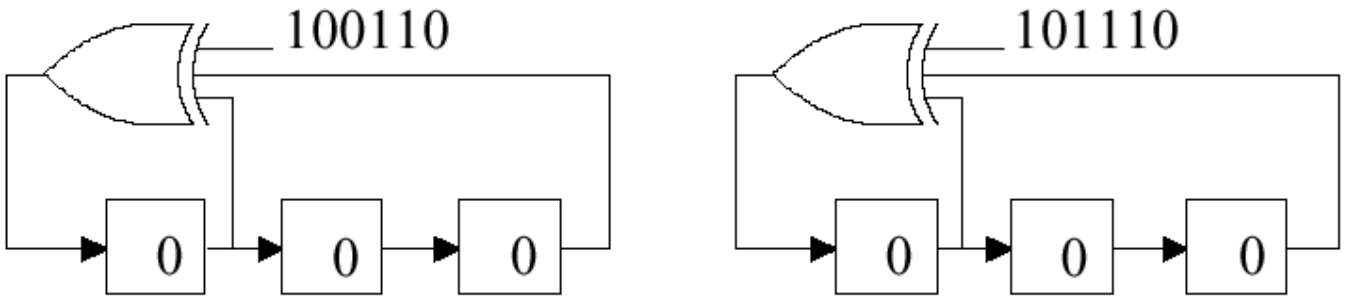
Pseudo-Random Pattern Generator



1	0	0
1	1	0
1	1	1
0	1	1
1	0	1
0	1	0

Fig. 9.23 Linear feedback shift register as a pseudo-random pattern generator.

Signature Analyzer



1	0	0	1	0	0
1	1	0	1	1	0
1	1	1	0	1	1
1	1	1	0	0	1
1	1	1	0	0	0
0	1	1	0	0	0

Fig. 9.24 Signature analyzer.

Test Setup

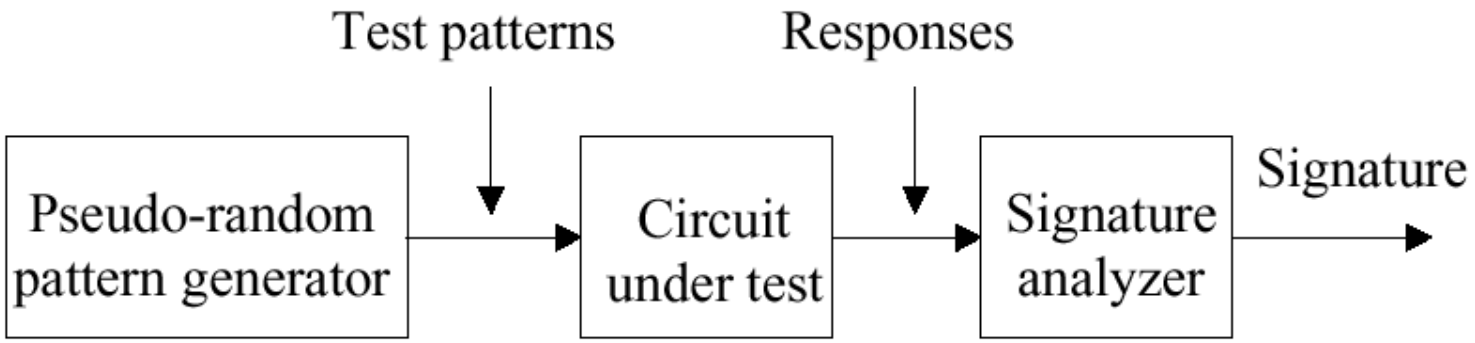


Fig. 9.25 Setup of a pseudo-random pattern generator and a signature analyzer to test a circuit.

Problem 9.3

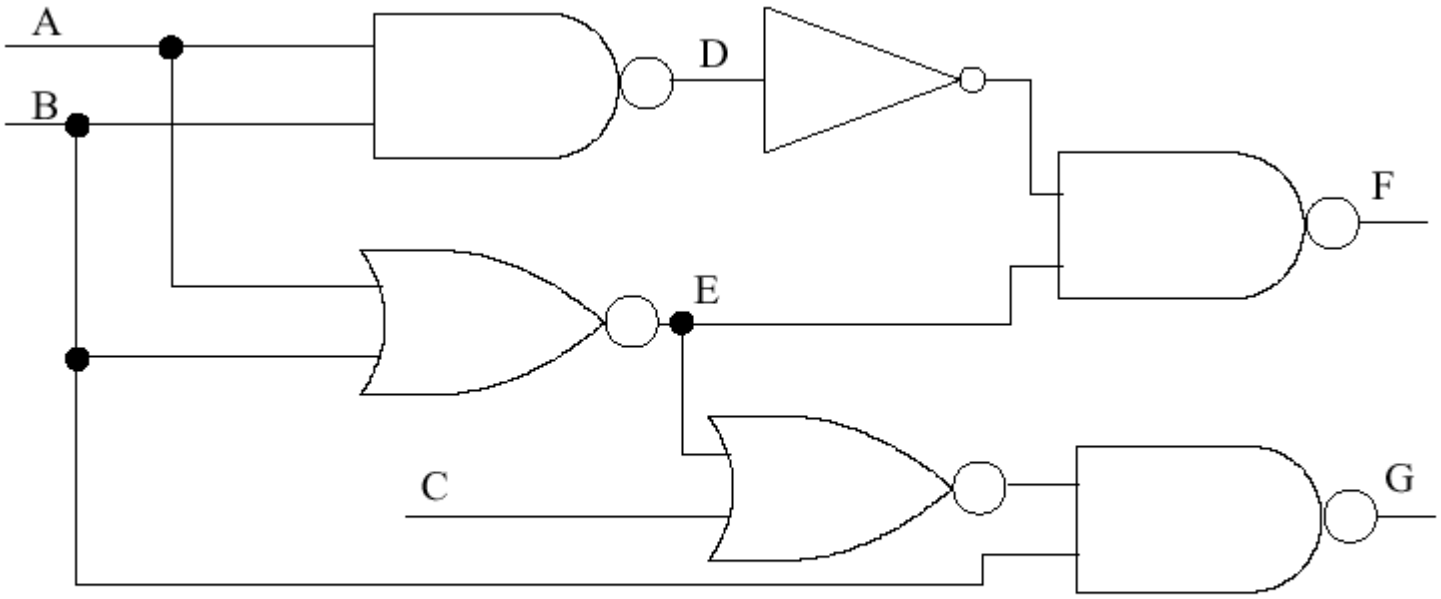


Fig. 9.26 Circuit for Problem 9.3.