Chapter 13

Fault Tolerant VLSI Architectures

System Reliability

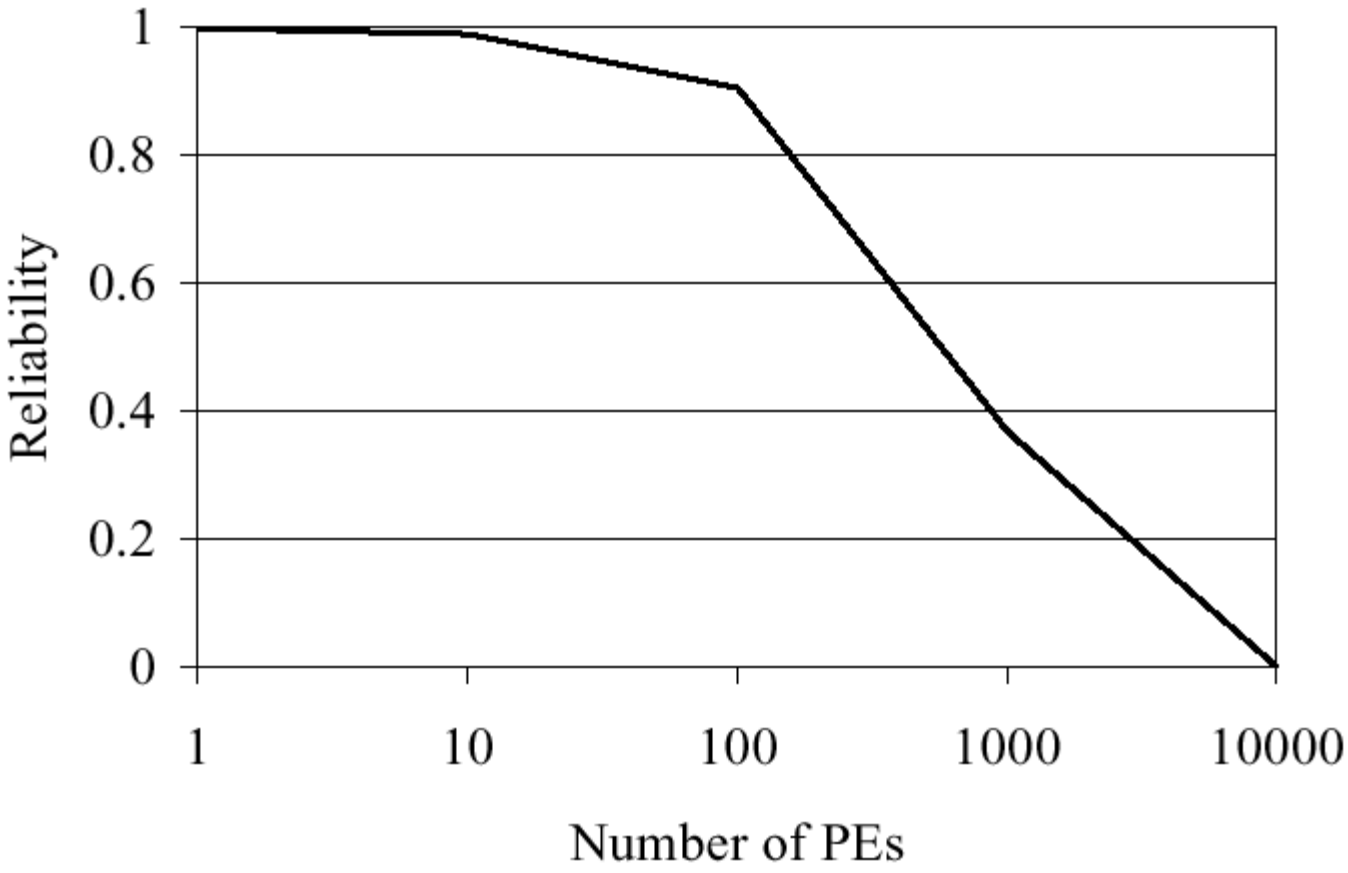

Fig. 13.1 Reliability of a system with multiple PEs.

Failure Rate Curve

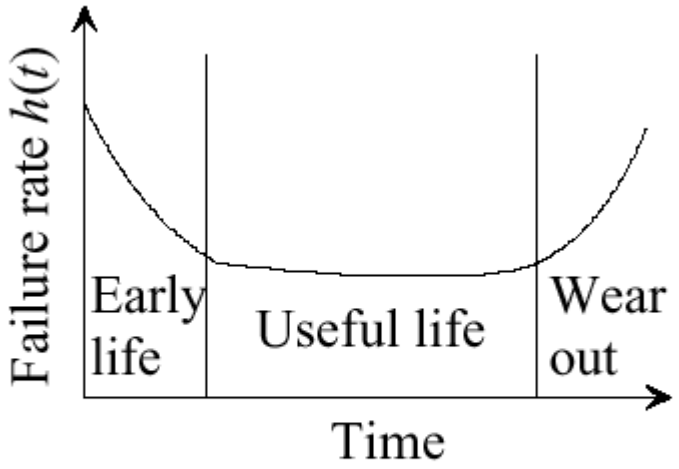

Fig. 13.2 A typical failure rate curve.

TMR System

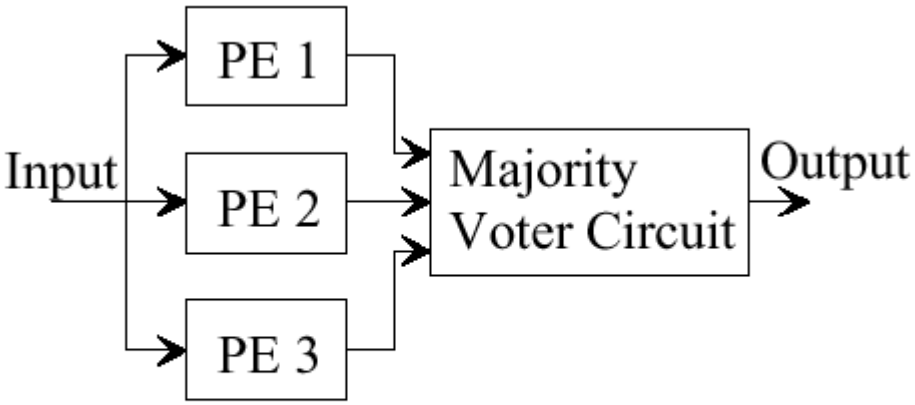

Fig. 13.3 A TMR system.

Fault Tolerant Array

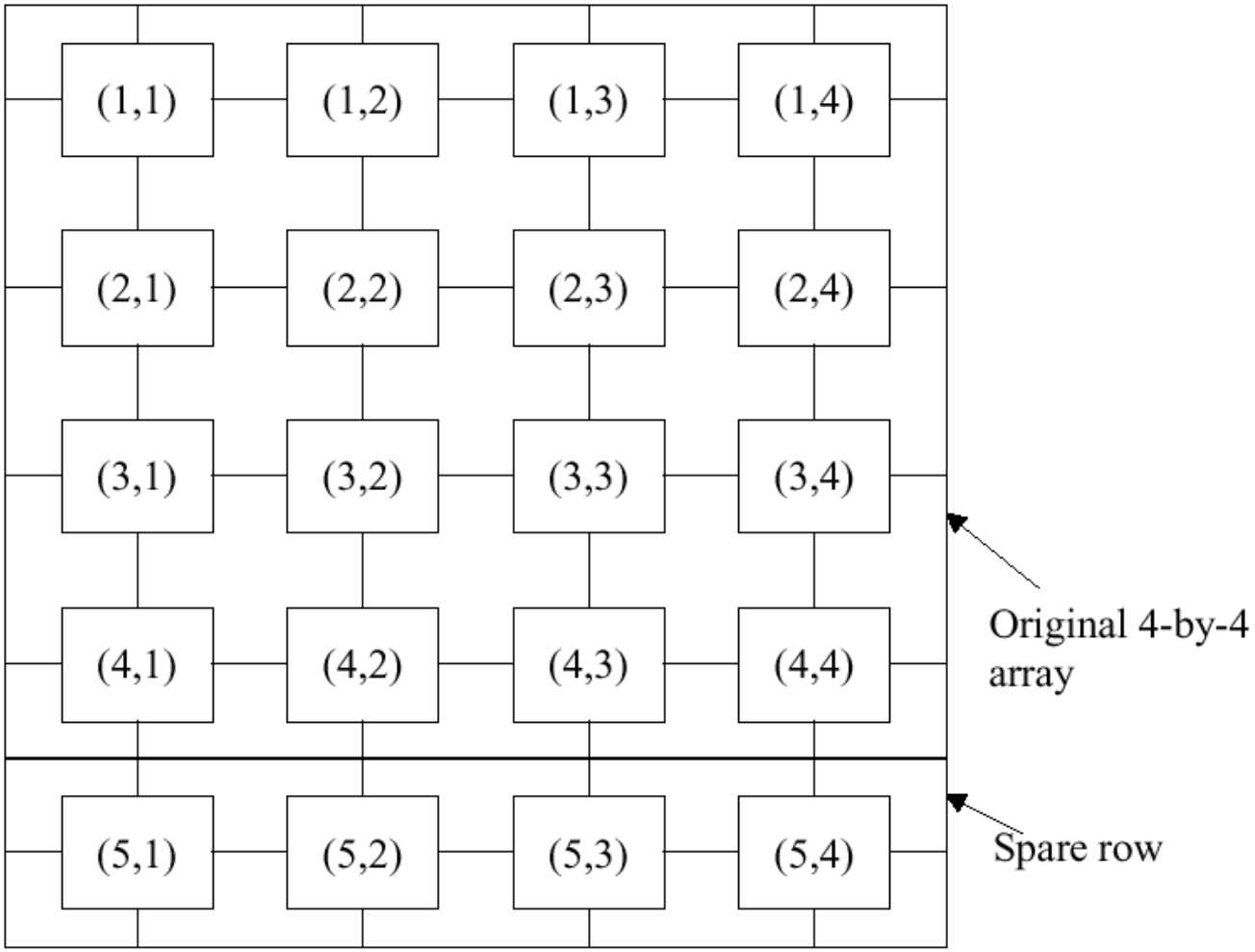

Fig. 13.4 5×4 fault tolerant array processor.

Set Replacement

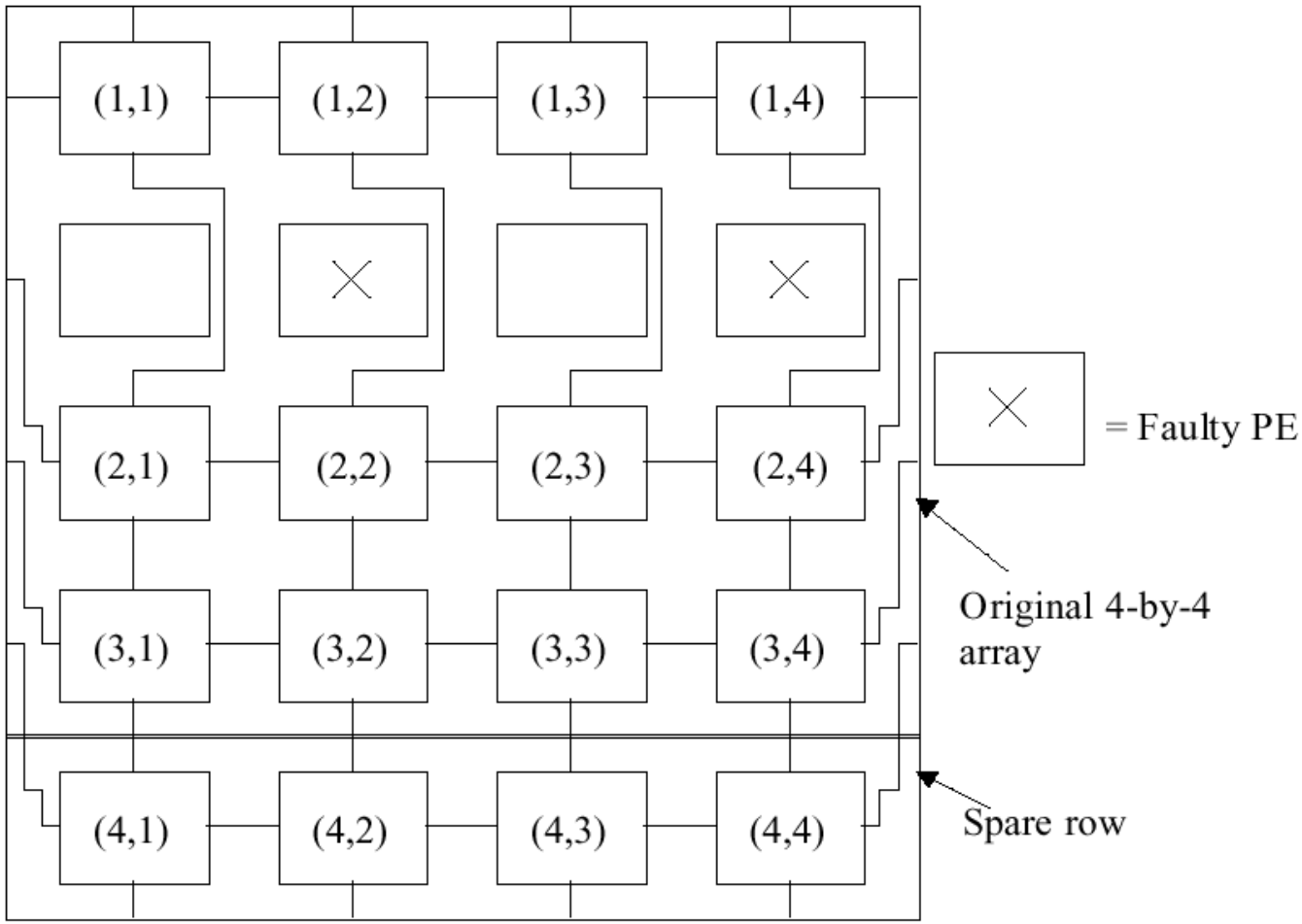

Fig. 13.5 Array reconfigured using the set replacement algorithm.

Reconfigurable Routing Structure

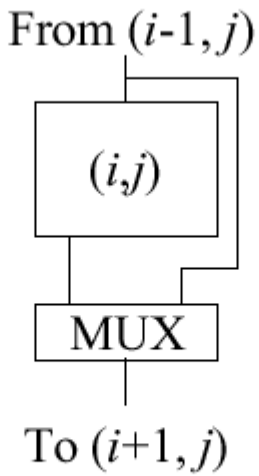

Fig. 13.6 Reconfigurable routing structure for set replacement algorithm.

Fault Tolerant Array

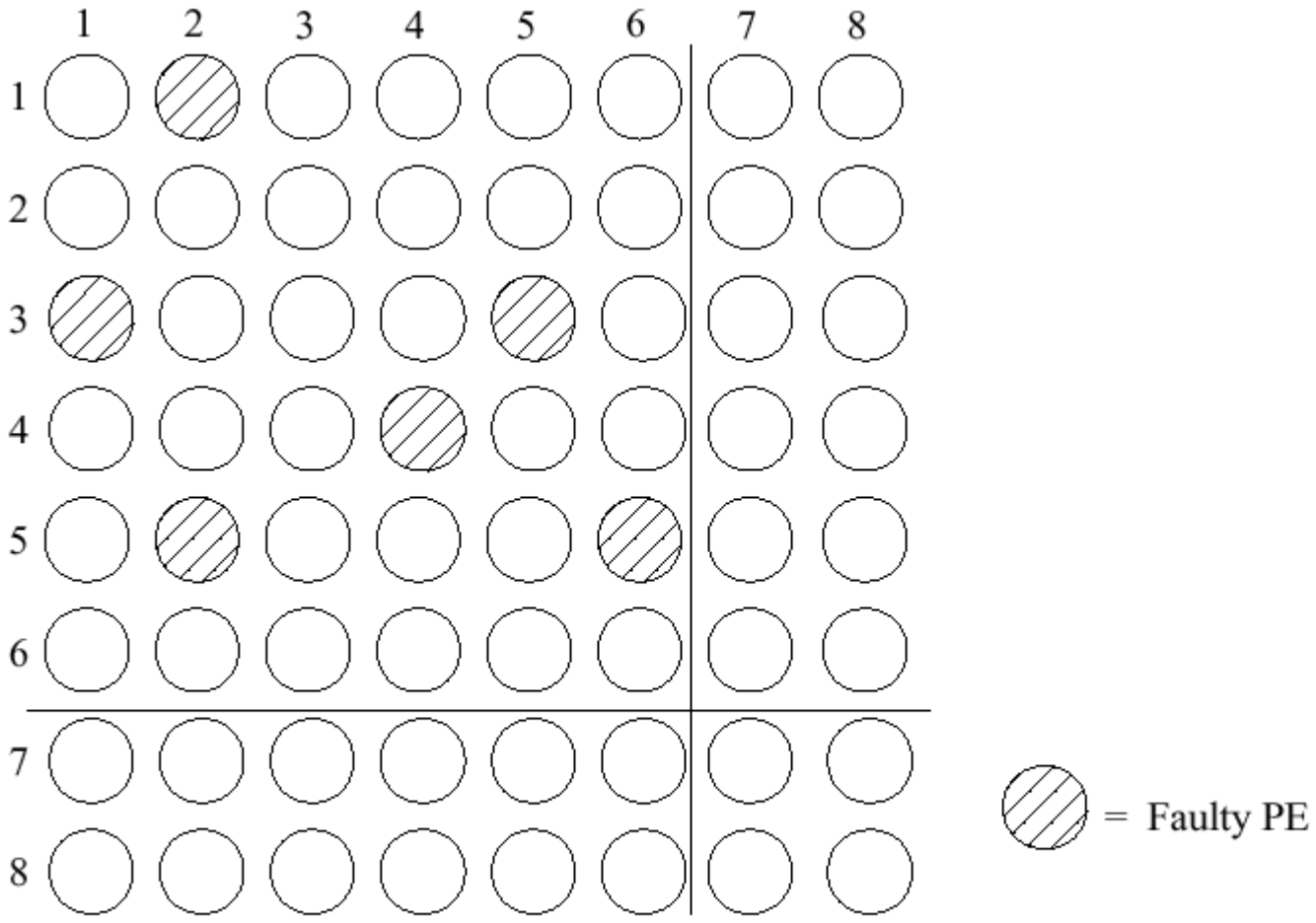

Fig. 13.7 A (6 + 2) × (6 + 2) fault tolerant array.

Bipartite Graph

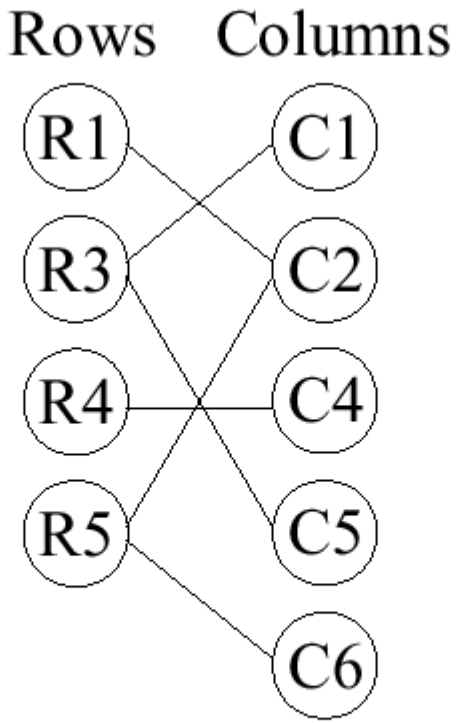

Fig. 13.8 Bipartite graph for reconfiguring the array in Fig. 13.7.

Shifting Replacement

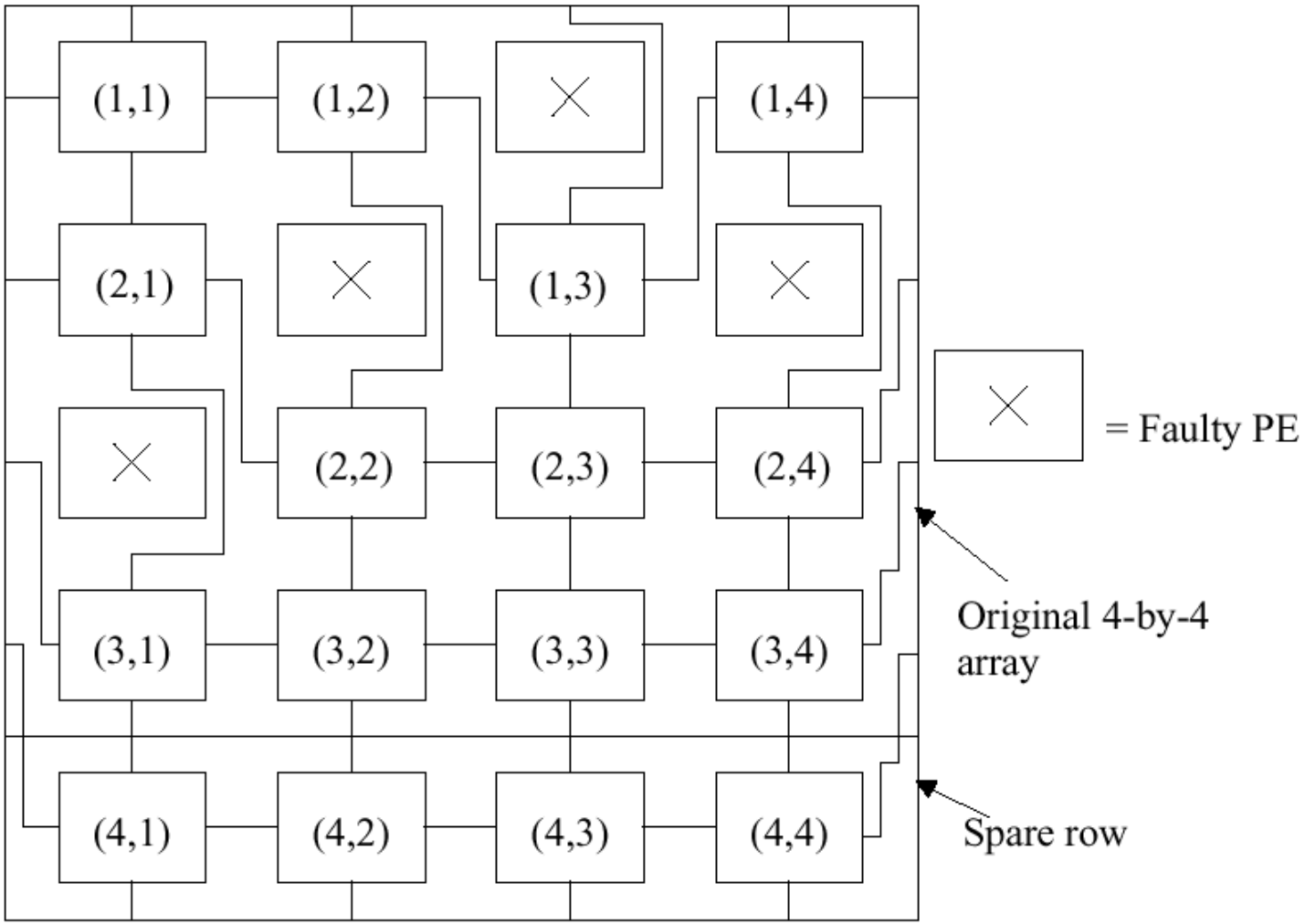

Fig. 13.9 Shifting replacement algorithm.

Routing Structure

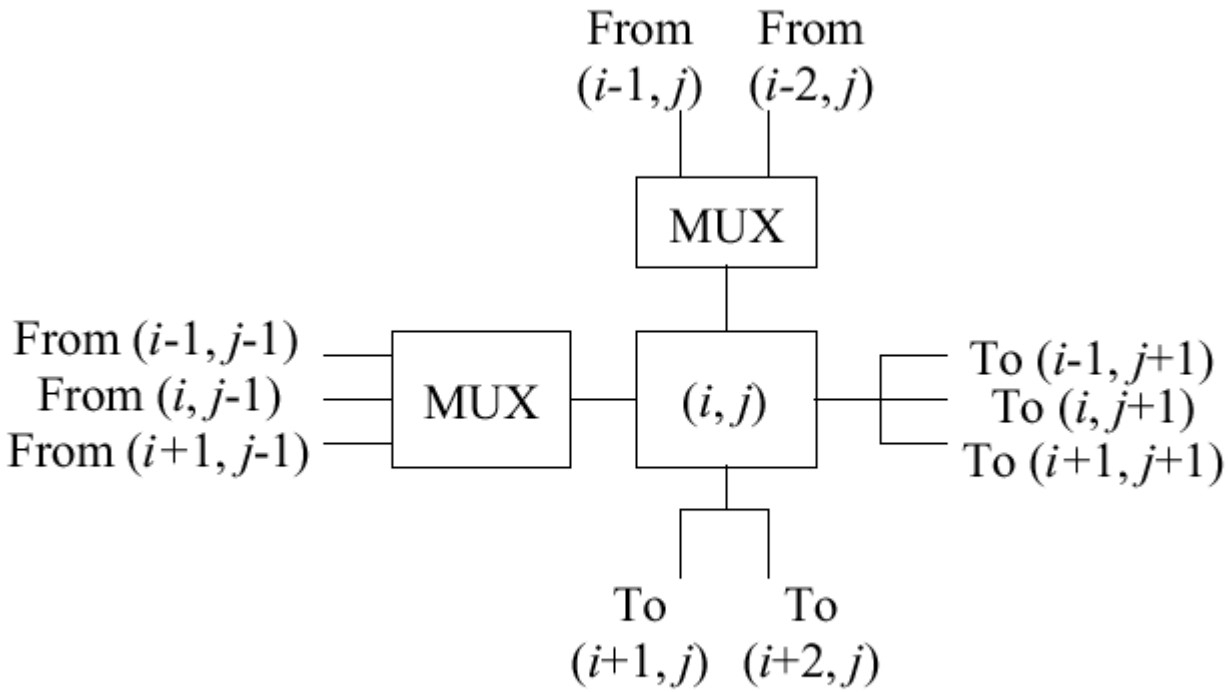

Fig. 13.10 Routing structure for the shifting replacement algorithm.

Augmented Array

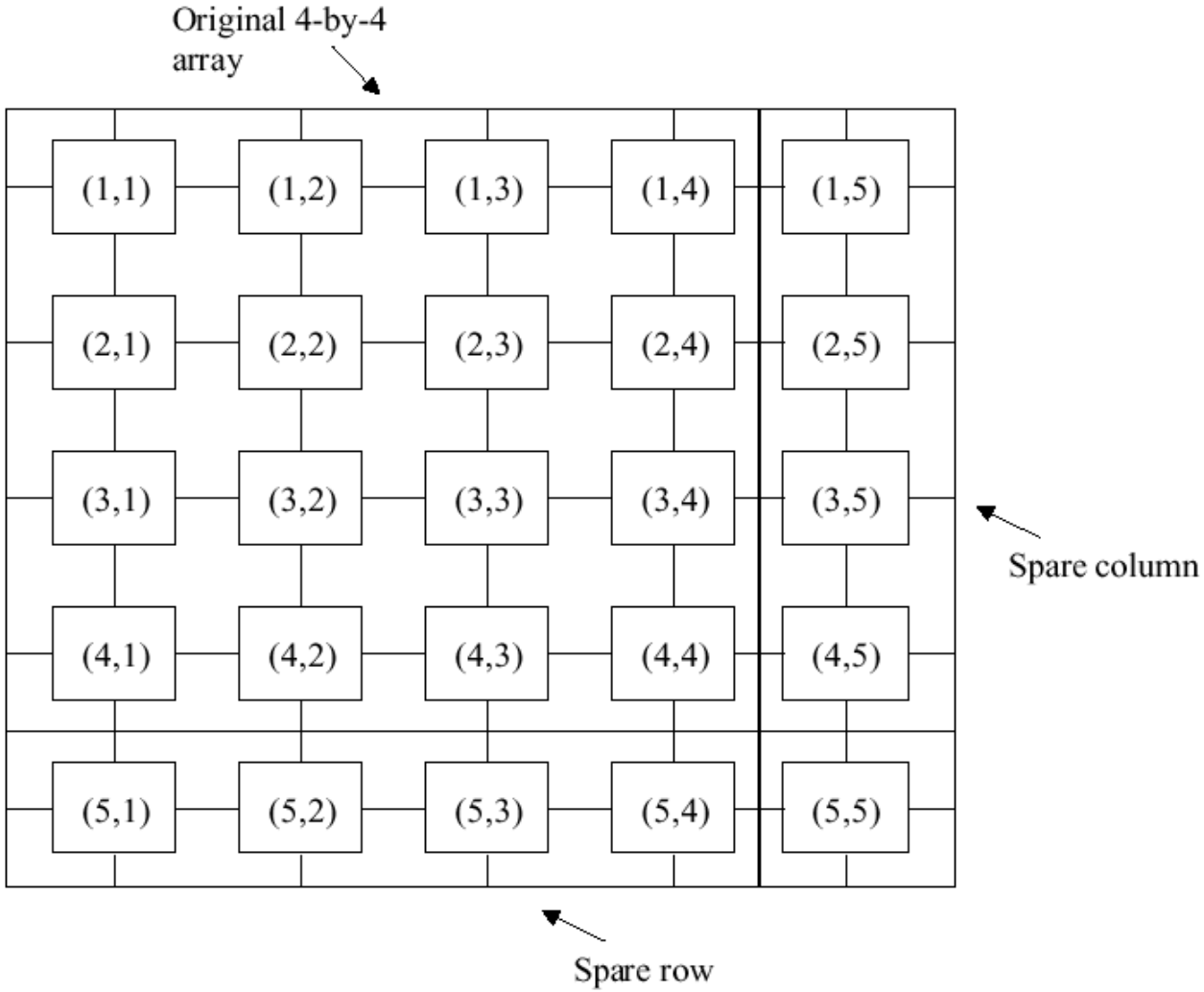

Fig. 13.11 4×4 array augmented with one spare column and one spare row.

Direct Reconfiguration

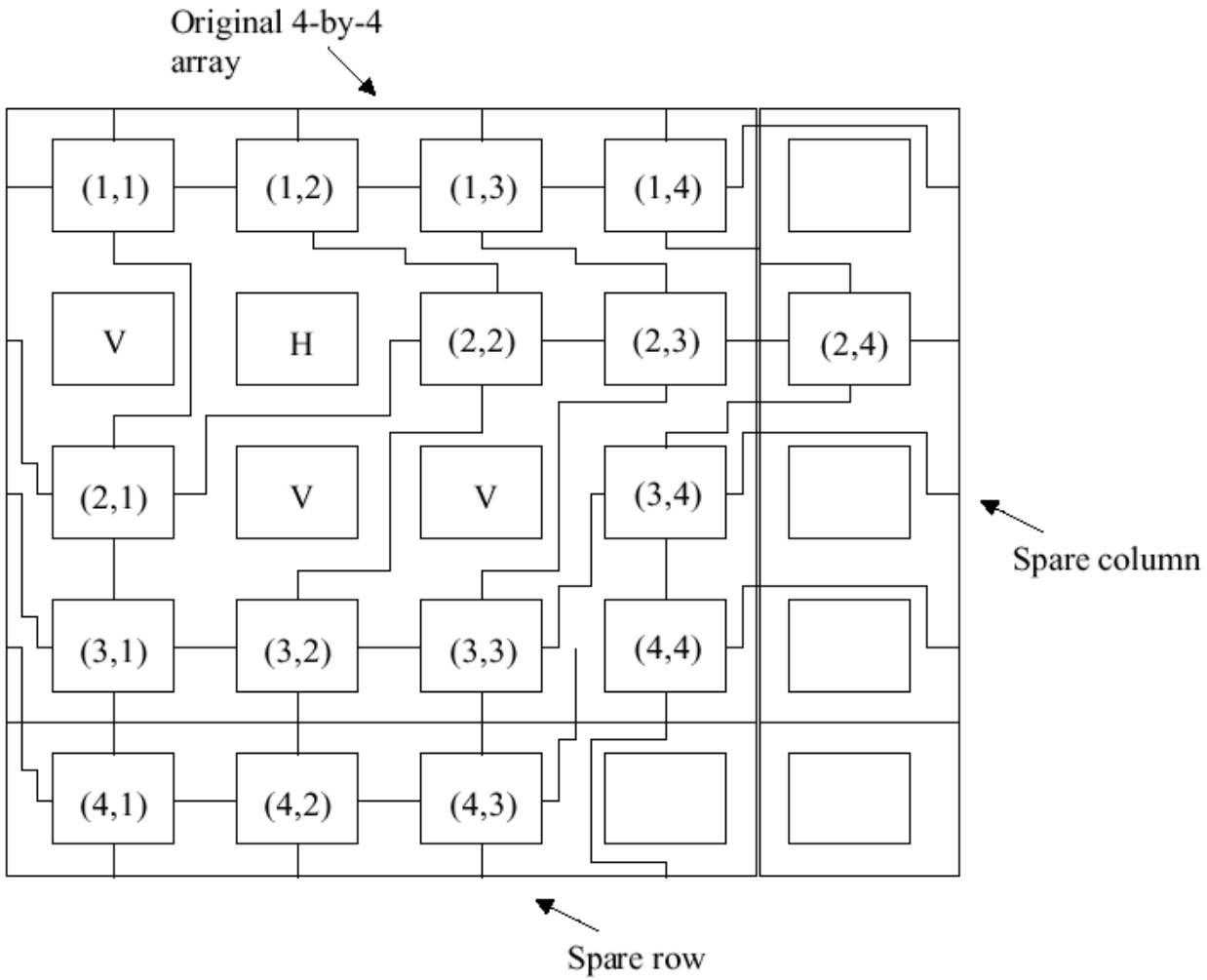

Fig. 13.12 Direct reconfiguration.

Complex Fault Stealing

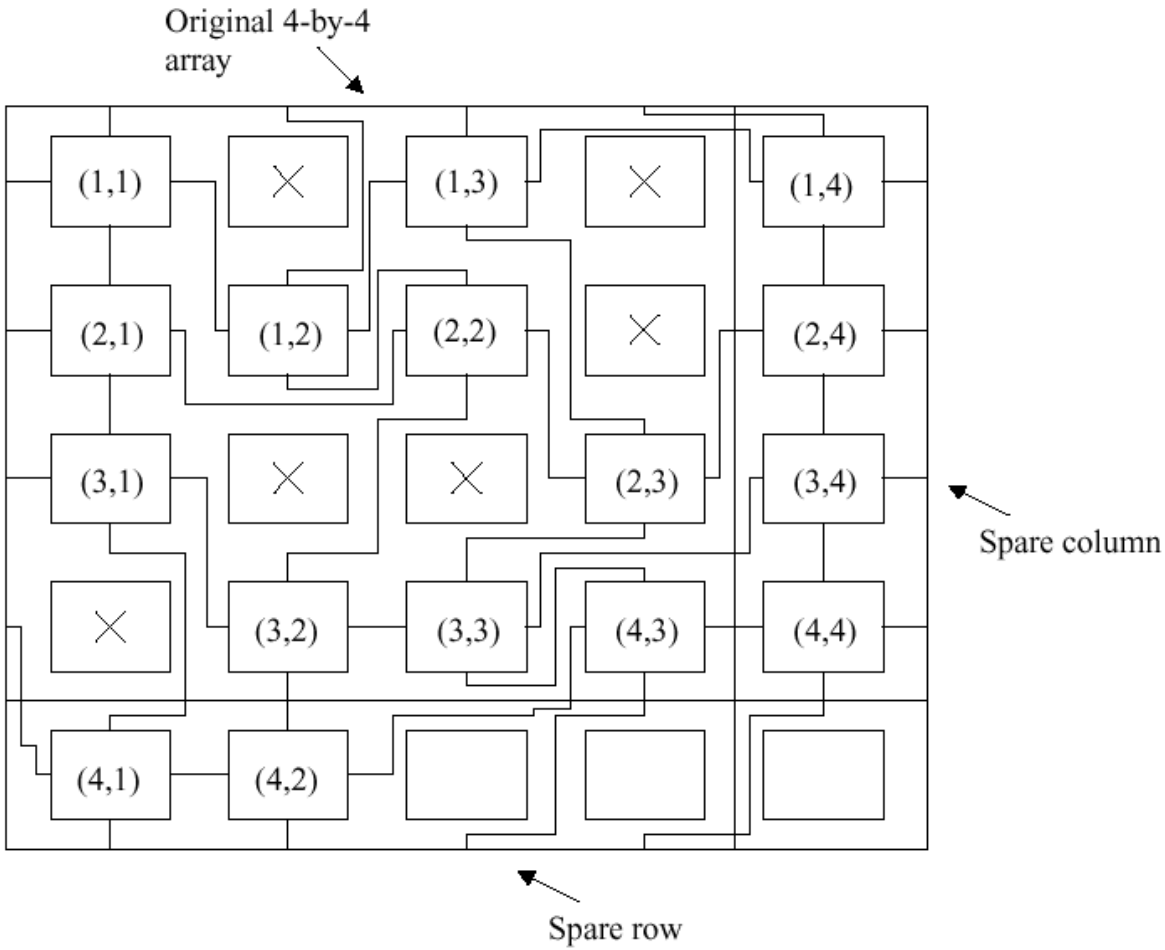

Fig. 13.13 Complex fault stealing algorithm.

Compensation Path Replacement

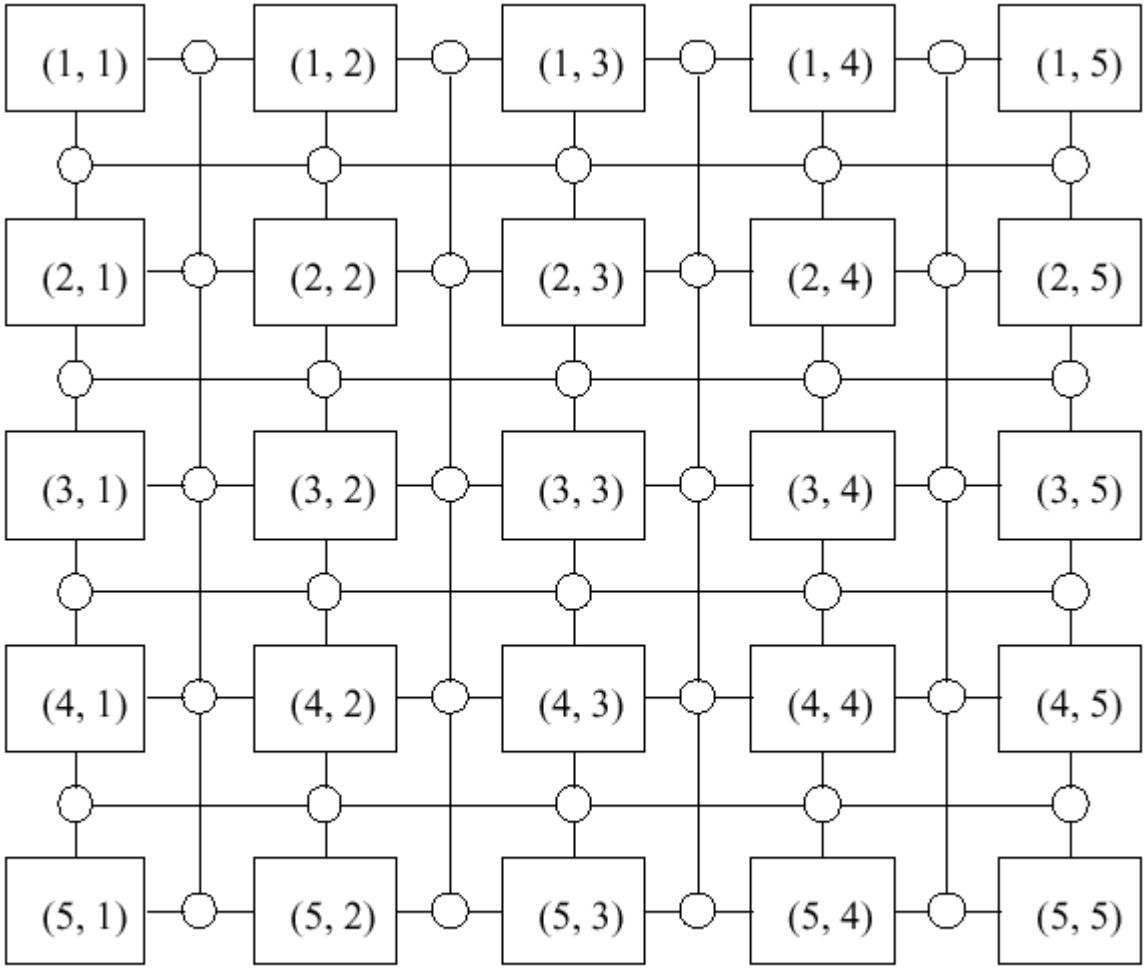

Fig. 13.14 Fault tolerant array for compensation path replacement algorithm.

Routing Switches

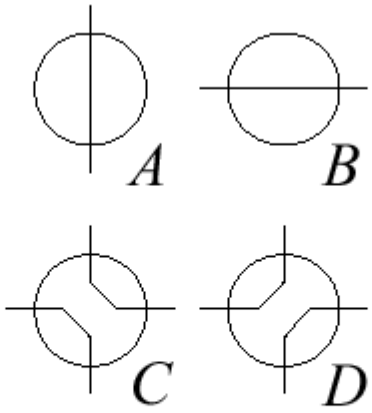

Fig. 13.15 Four states of the routing switches used in Fig. 13.14.

Compensation Paths

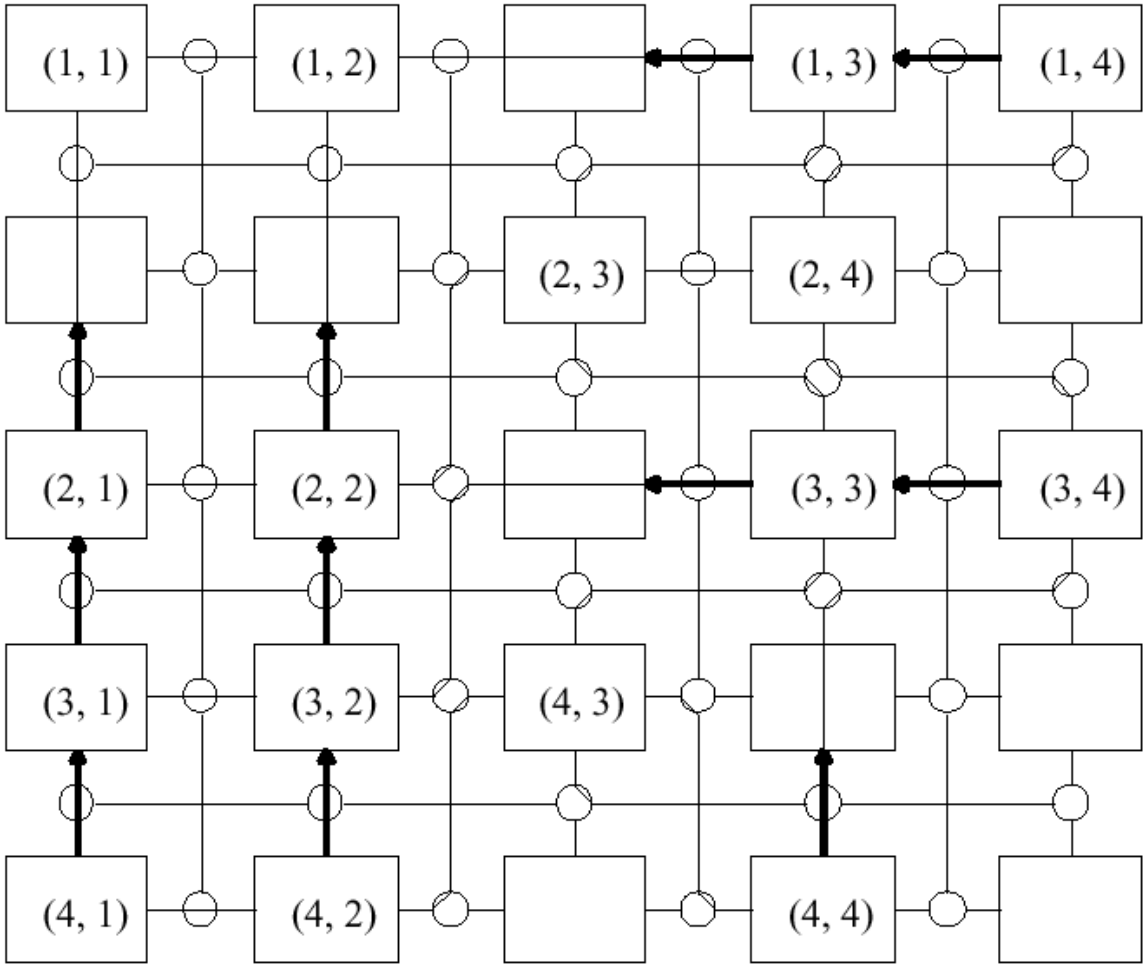

Fig. 13.16 Reconfiguration using compensation paths.