Chapter 4

CMOS Circuit Characterization

NMOS Characteristics

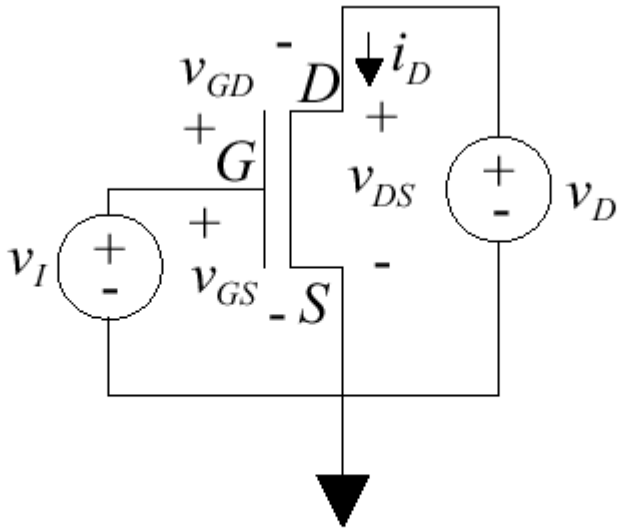

Fig. 4.1 Setup for measuring the i_D-v_{DS} characteristics of an nMOS transistor.

NMOS Characteristics

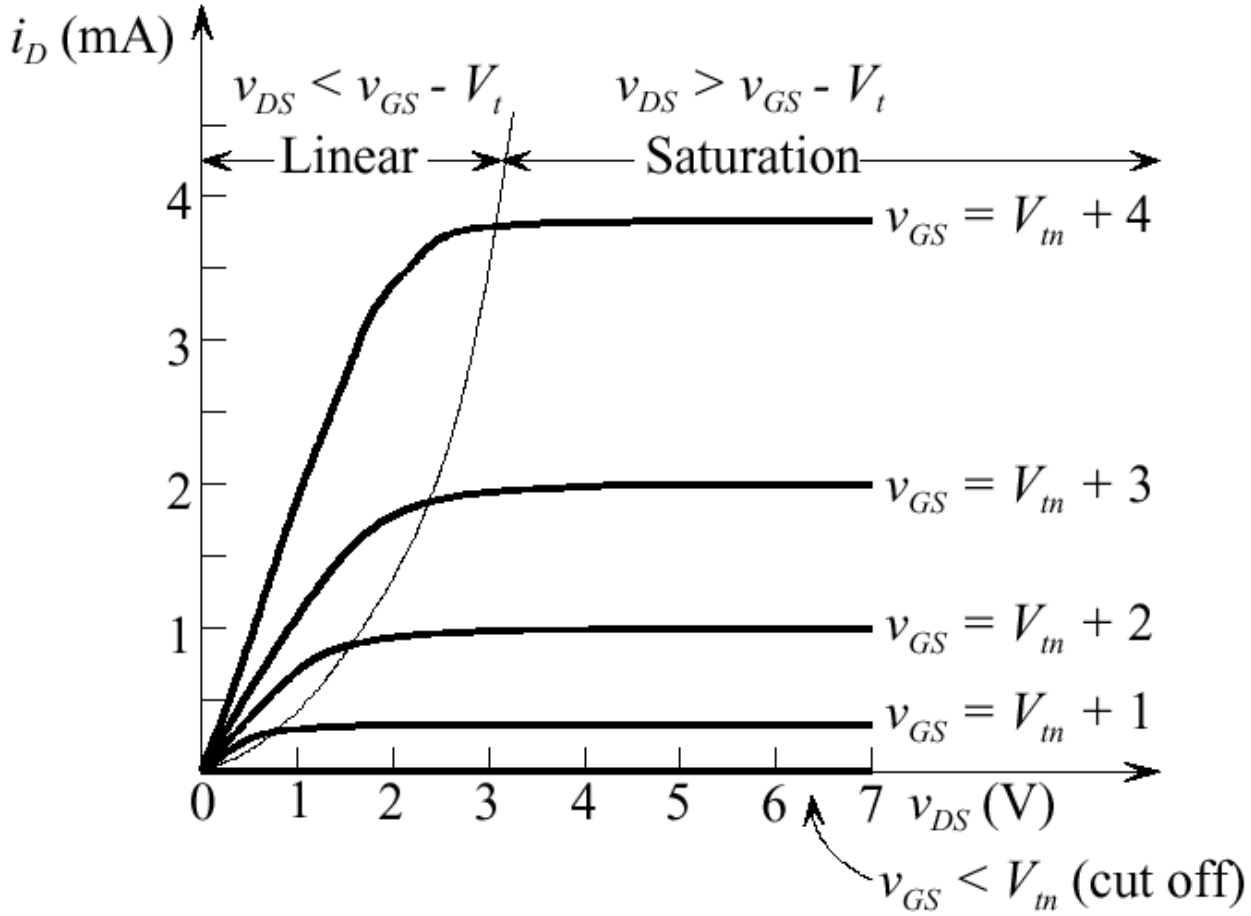

Fig. 4.2 The i_D-v_{DS} characteristics for the nMOS transistor.

PMOS Characteristics

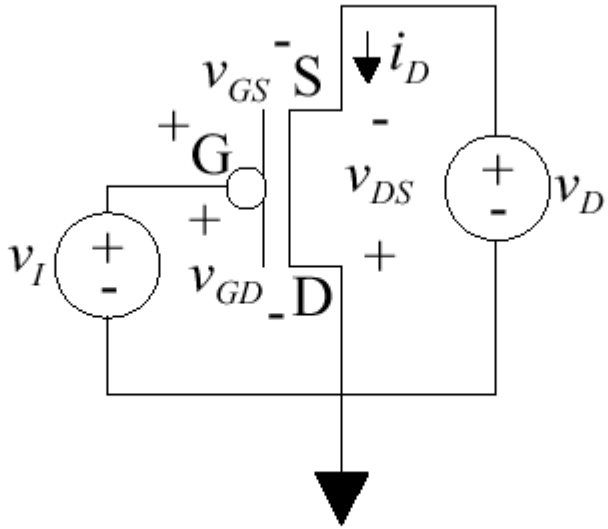

Fig. 4.3 Setup for measuring the i_D-v_{DS} characteristics of a pMOS transistor.

Operation Regions

Operating Regions	nMOS ($v_{GS} > 0, v_{DS} > 0, V_{tn} > 0$)	pMOS ($v_{GS} < 0, v_{DS} < 0, V_{tp} < 0$)
Cutoff	$v_{GS} \le V_{tn}, i_D = 0$	$v_{GS} \ge V_{tp}, i_D = 0$
Linear	$v_{GS} > V_{tn}$ $v_{DS} < v_{GS} - V_{tn}$ $i_D = k_n \frac{W}{L}\left[(v_{GS} - V_{tn})v_{DS} - \frac{1}{2}v_{DS}^2\right]$	$v_{GS} < V_{tp}$ $v_{DS} > v_{GS} - V_{tp}$ $i_D = k_p \frac{W}{L}\left[(v_{GS} - V_{tp})v_{DS} - \frac{1}{2}v_{DS}^2\right]$
Saturation	$v_{GS} > V_{tn}$ $v_{DS} > v_{GS} - V_{tn}$ $i_D = \frac{1}{2}k_n \frac{W}{L}(v_{GS} - V_{tn})^2$	$v_{GS} < V_{tp}$ $v_{DS} < v_{GS} - V_{tp}$ $i_D = \frac{1}{2}k_p \frac{W}{L}(v_{GS} - V_{tp})^2$

Fig. 4.4 Operation regions of nMOS and pMOS transistors.

Inverter Voltage Transfer

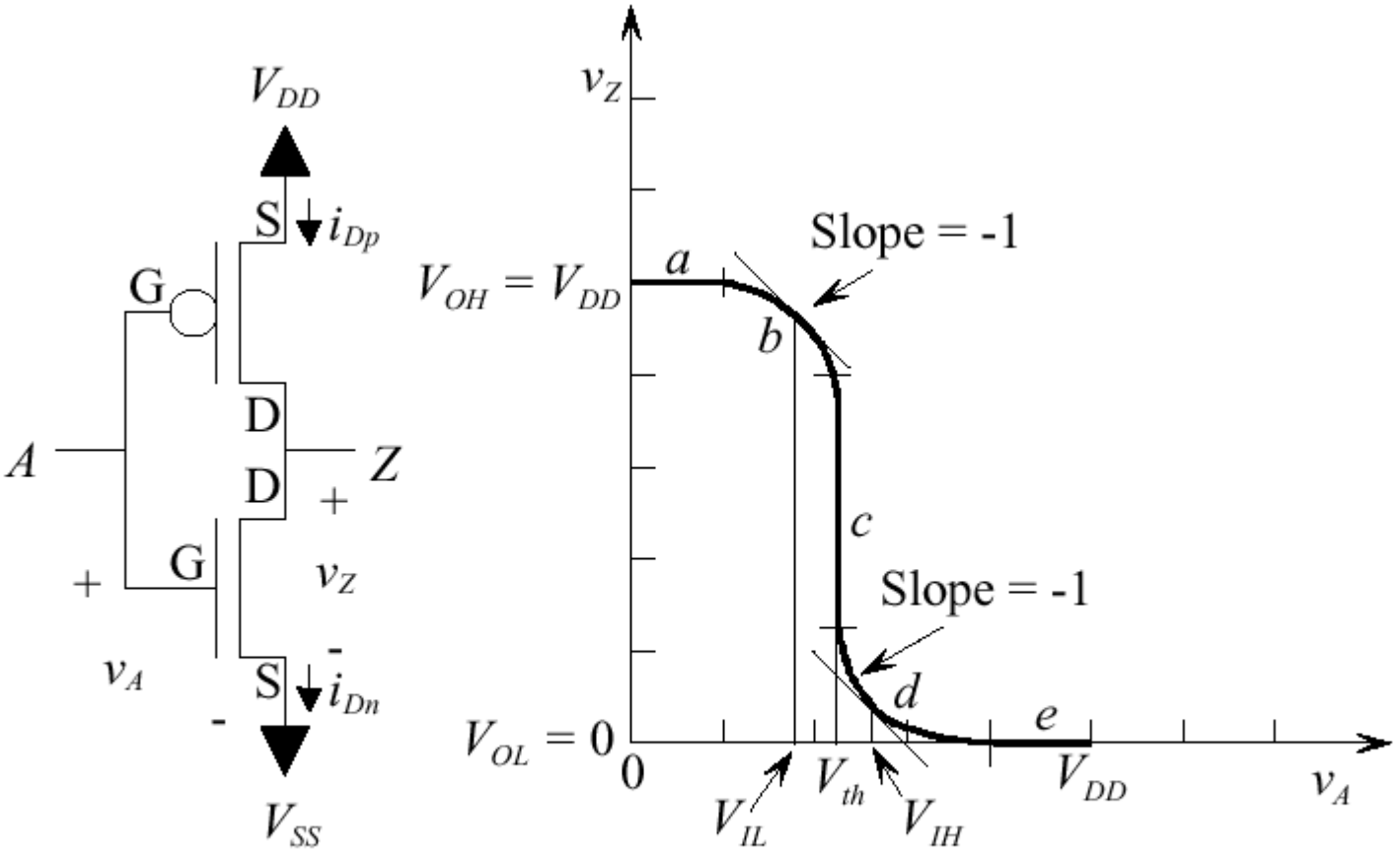

Fig. 4.5 CMOS inverter and its voltage transfer characteristic.

Operation Regions

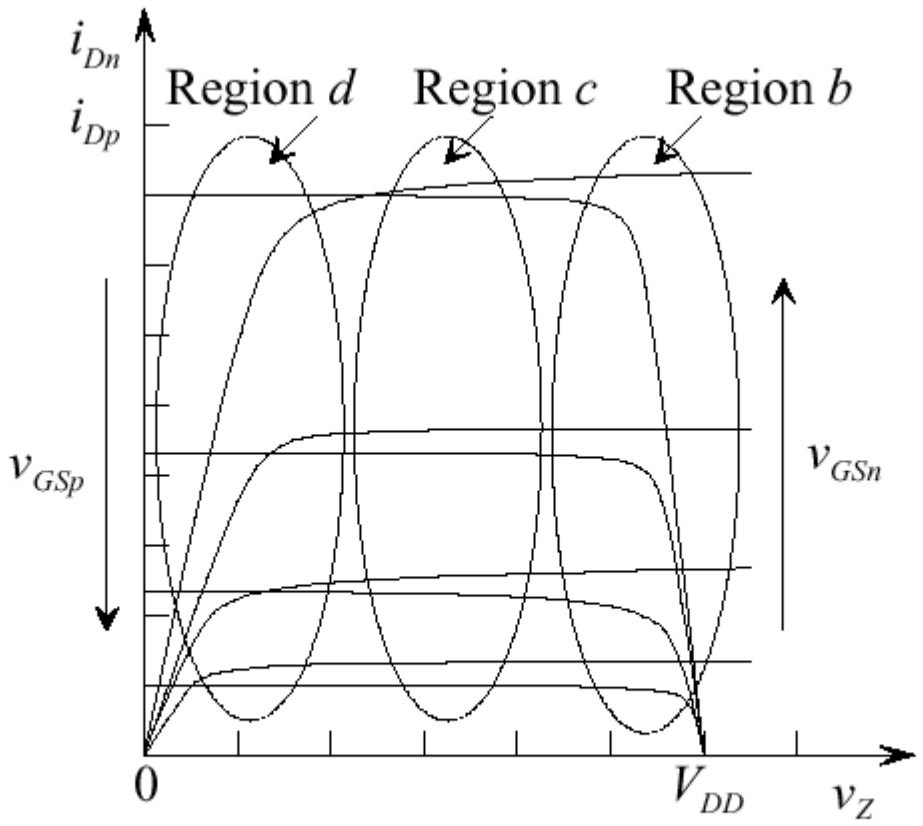

Fig. 4.6 Relationship between the nMOS and pMOS transistors in an inverter.

Spice Model

```
.MODEL nfet NMOS LEVEL=2 LD=0.12U TOX=200E-10
+NSUB=1.0E+16 VTO=0.8 KP=5.0E-5 GAMMA=0.45 PHI=0.6
+UO=700 VMAX=70000 XJ=0.6U LAMBDA=.02 NSS=0.0
+TPG=1.00 RSH=0 CGSO=0.9E-10 CGDO=0.9E-10 CJ=1.4E-4
+MJ=0.6 CJSW=6.5E-10 MJSW=0.3

.MODEL pfet PMOS LEVEL=2 LD=0.18U TOX=200E-10
+NSUB=1.5E+15 VTO=-0.7 KP=2.0E-5 GAMMA=0.45 PHI=0.6
+UO=250 VMAX=34600 XJ=0.4U LAMBDA=.04 NSS=0.0
+TPG=-1.00 RSH=0 CGSO=1.4E-10 CGDO=1.4E-10 CJ=2.4E-4
+MJ=0.5 CJSW=3.5E-10 MJSW=0.3
```

Spice Deck

```
* SPICE DECK created for a CMOS inverter Z=not(A)

M1 1 2 3 1 pfet L=1.0U W=4.0U
M2 3 2 0 0 nfet L=1.0U W=4.0U
C3 3 0 0.028000PF

*  A   2
*  GND 0
*  VDD 1
*  Z   3

* CMOS SPICE model parameters

.MODEL nfet NMOS LEVEL=2 LD=0.12U TOX=200E-10
+NSUB=1.0E+16 VTO=0.8 KP=5.0E-5 GAMMA=0.45 PHI=0.6
+UO=700 VMAX=70000 XJ=0.6U LAMBDA=.02 NSS=0.0
+TPG=1.00 RSH=0 CGSO=0.9E-10 CGDO=0.9E-10 CJ=1.4E-4
+MJ=0.6 CJSW=6.5E-10 MJSW=0.3
```

Spice Deck

```
.MODEL pfet PMOS LEVEL=2 LD=0.18U TOX=200E-10
+NSUB=1.5E+15 VTO=-0.7 KP=2.0E-5 GAMMA=0.45 PHI=0.6
+UO=250 VMAX=34600 XJ=0.4U LAMBDA=.04 NSS=0.0
+TPG=-1.00 RSH=0 CGSO=1.4E-10 CGDO=1.4E-10 CJ=2.4E-4
+MJ=0.5 CJSW=3.5E-10 MJSW=0.3

* Power source
vps 1 0 dc 5

* Input waveform
vA 2 0 dc 0 pwl(0ns 0 0.01ns 5 10ns 5
+10.01ns 0 20ns 0 20.01ns 5 30ns 5)

* Perform a transient analysis with a step size
* of .1 ns for the duration of 40 ns.
.tran 0.1ns 40ns

* Provide values and plots for V(A) and V(Z)
.print tran v(2) v(3)
.plot tran v(2) v(3)

.end
```

Spice Simulation

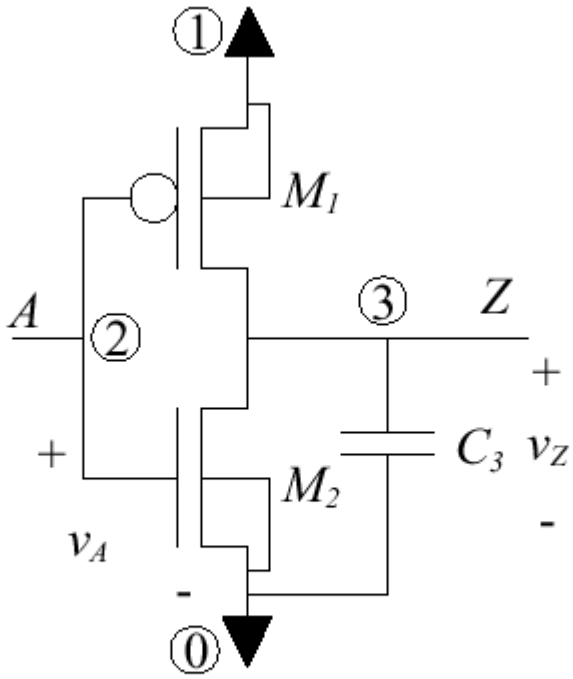

Fig. 4.7 Inverter circuit for SPICE simulation.

Spice Simulation

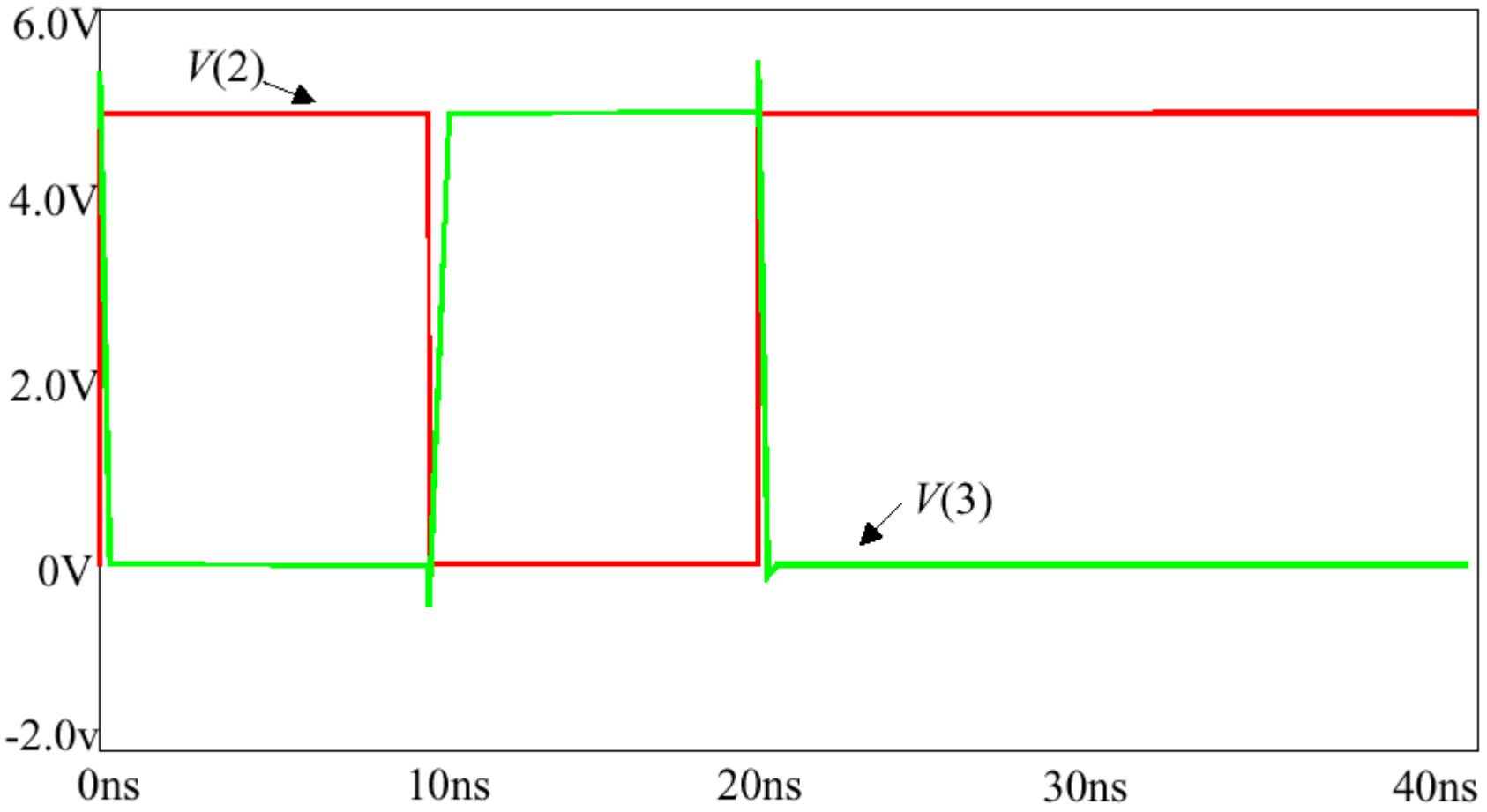

Fig. 4.8 SPICE simulation result of an inverter.

Resistive Switch Model

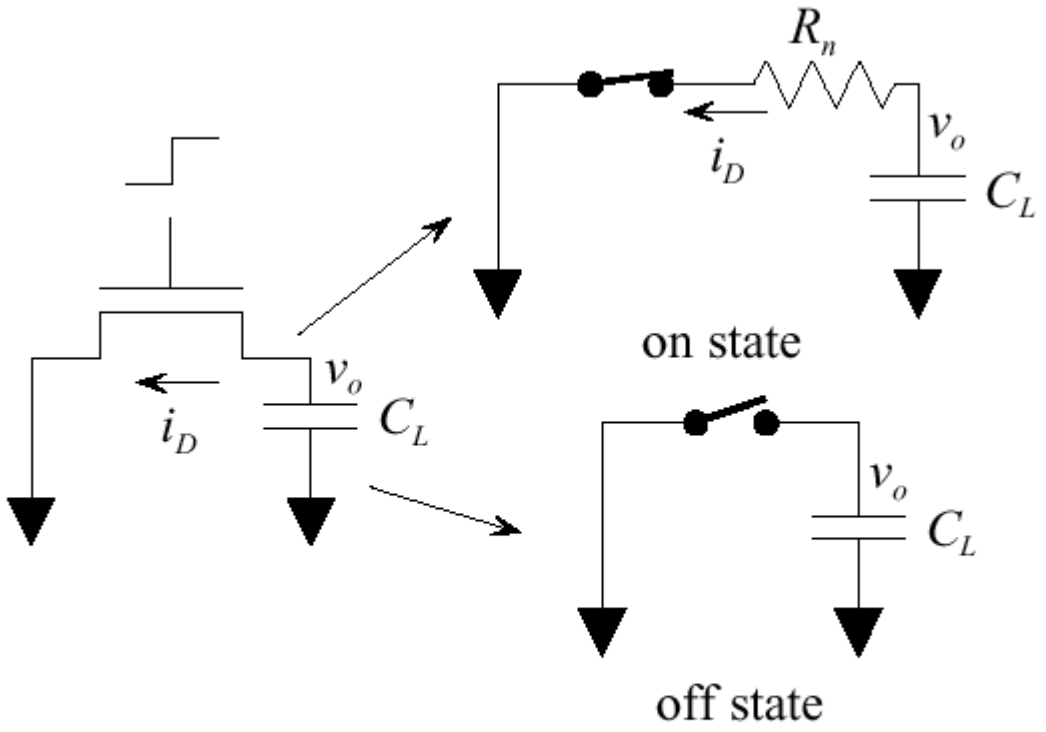

Fig. 4.9 Resistive switch model of an nMOS transistor.

Dynamic Behavior

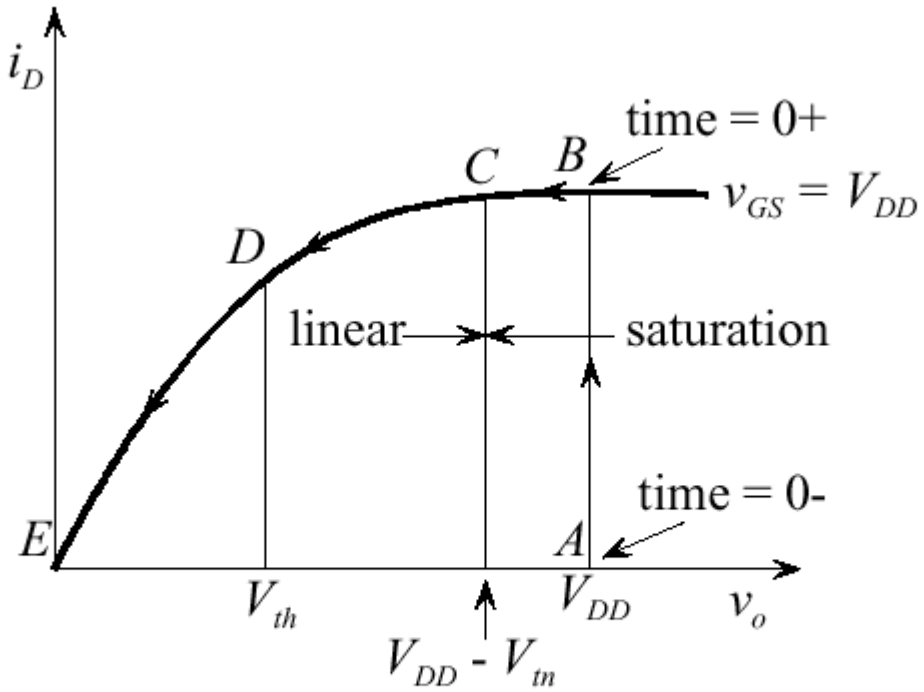

Fig. 4.10 Dynamic behavior of an nMOS transistor being turned on.

Propagation Delay

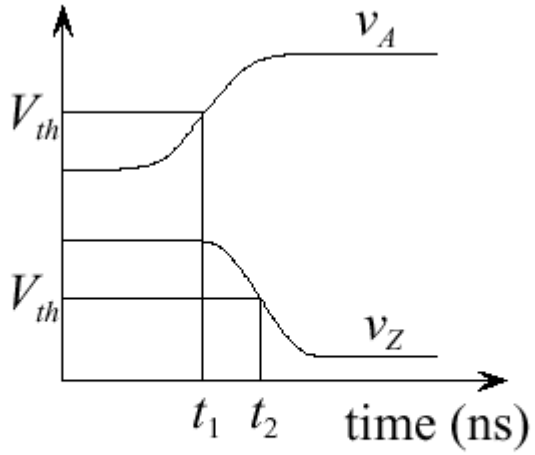

Fig. 4.11 Definition of propagation delay.

RC Timing Model

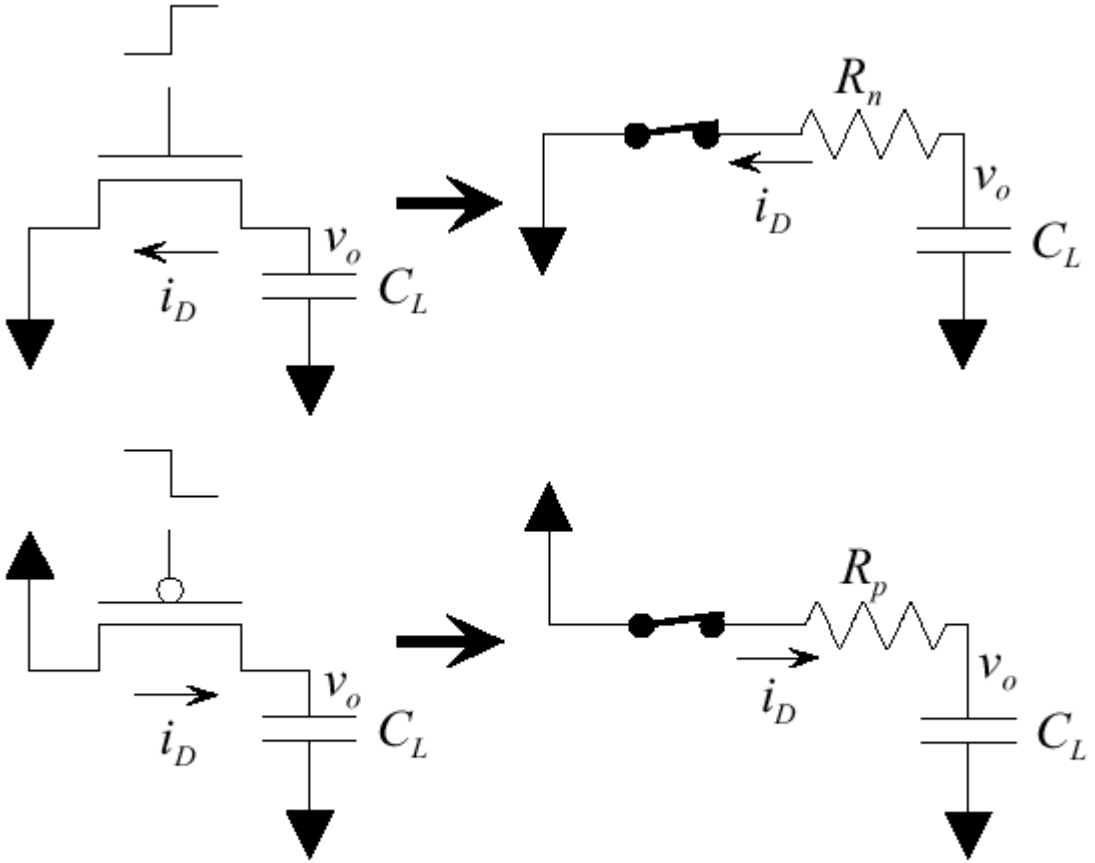

Fig. 4.12 RC timing models.

Resistance

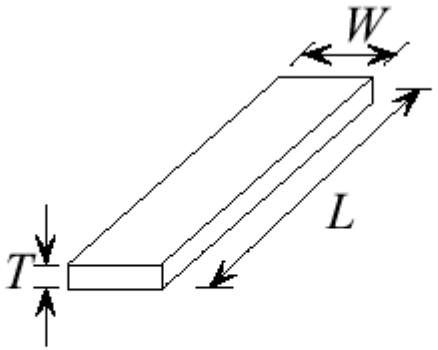

Fig. 4.13 Determination of resistance value.

Example Resistance and Capacitance

Layer	**Ω/square**
Metal 1 and 2	0.05
n-type Diffusion	2
p-type Diffusion	2
Polysilicon	4
nMOS Channel (effective)	6 K
pMOS Channel (effective)	15 K
Capacitance	**fF/μm^2**
nMOS and pMOS gate	1
Diffusion (area)	0.8
Diffusion (periphery)	0.3 (fF/μm)
Polysilicon	0.1
Metal 1	0.05
Metal 2	0.02

Fig. 4.14 Example resistance and capacitance values.

Resistance

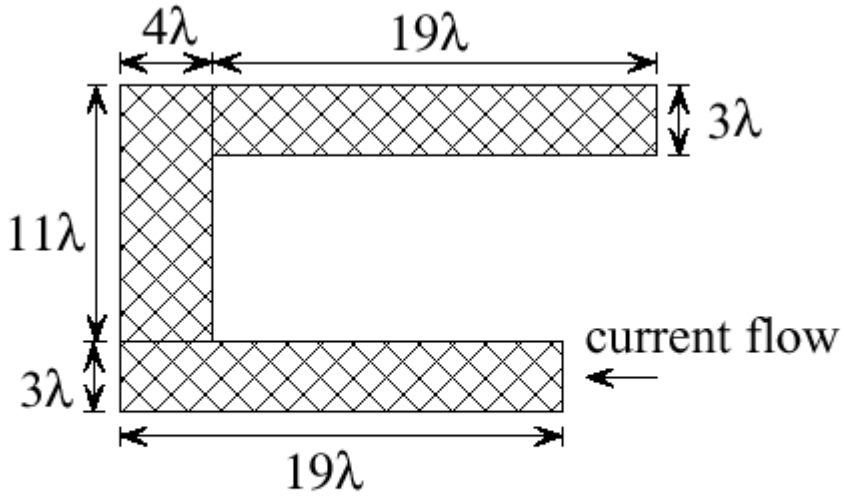

Fig. 4.15 Resistance value calculation of a polysilicon wire.

Capacitance

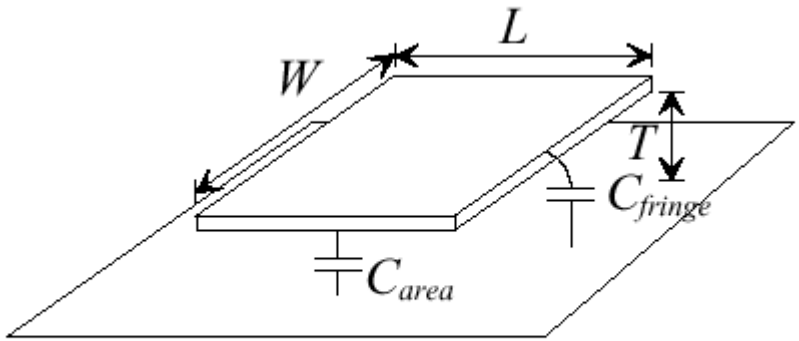

Fig. 4.16 Determination of capacitance value.

Diffusion Capacitance

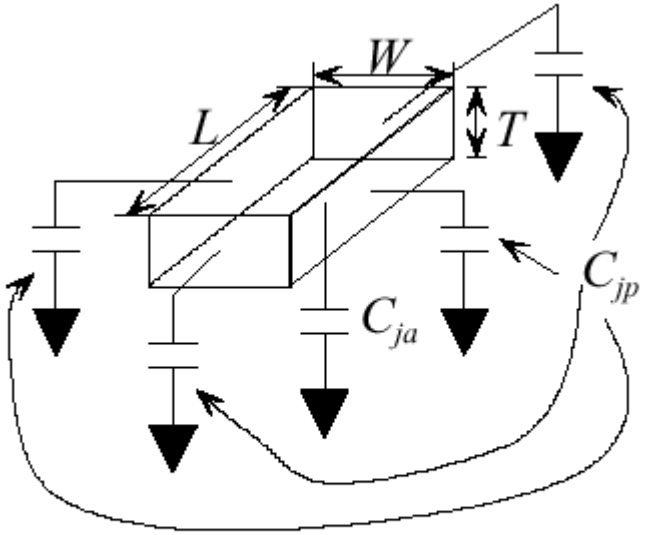

Fig. 4.17 Diffusion capacitance.

Resistance and Capacitance

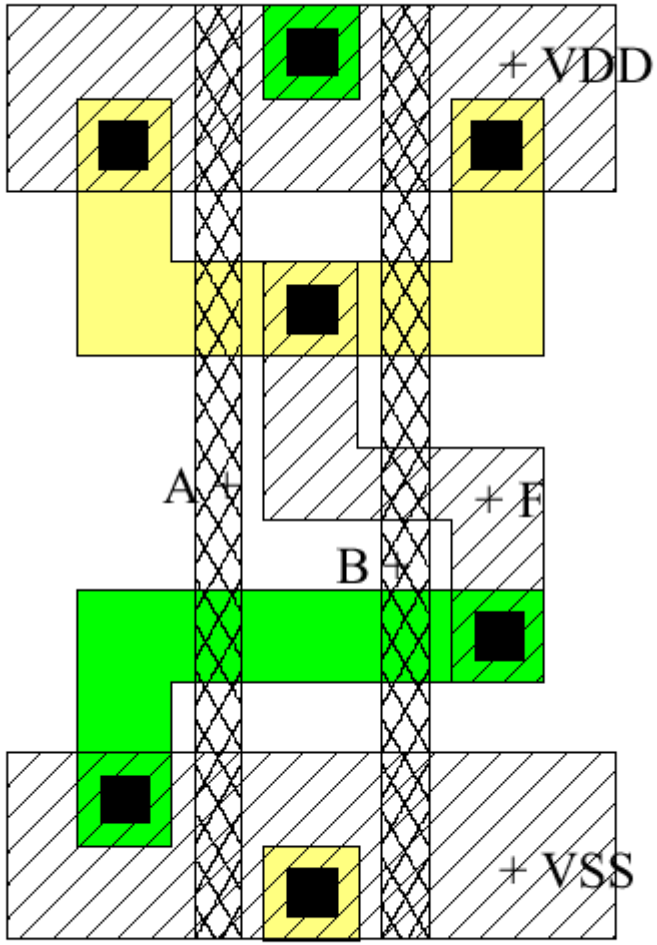

Fig. 4.18 Resistance and capacitance value estimation.

Wire Capacitance

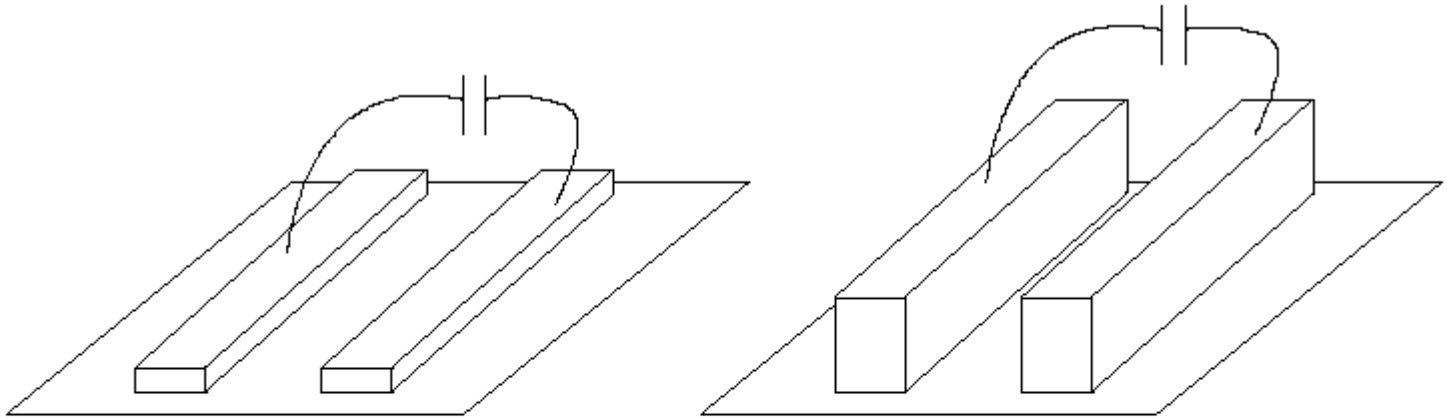

Fig. 4.19 Capacitance between two wires: (a) Before sub-micron; (b) Deep sub-micron.

RC Tree

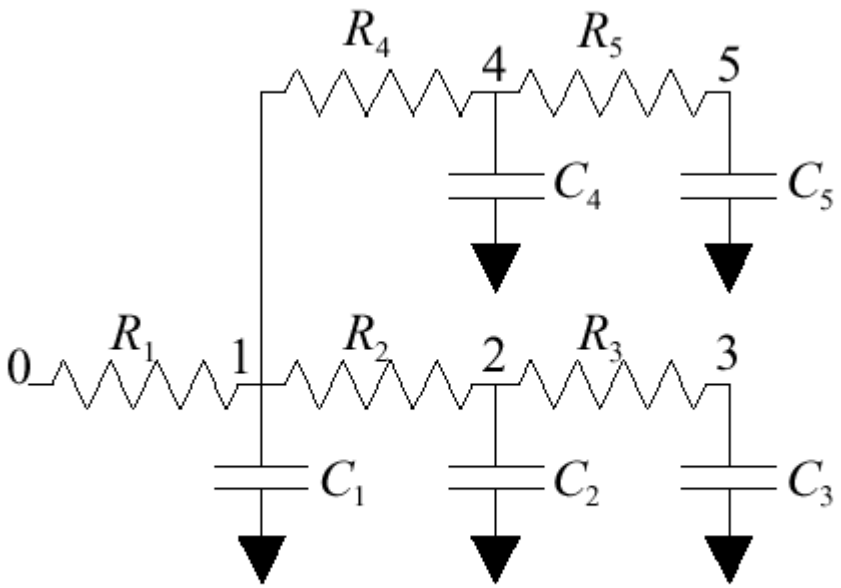

Fig. 4.20 RC tree.

Load

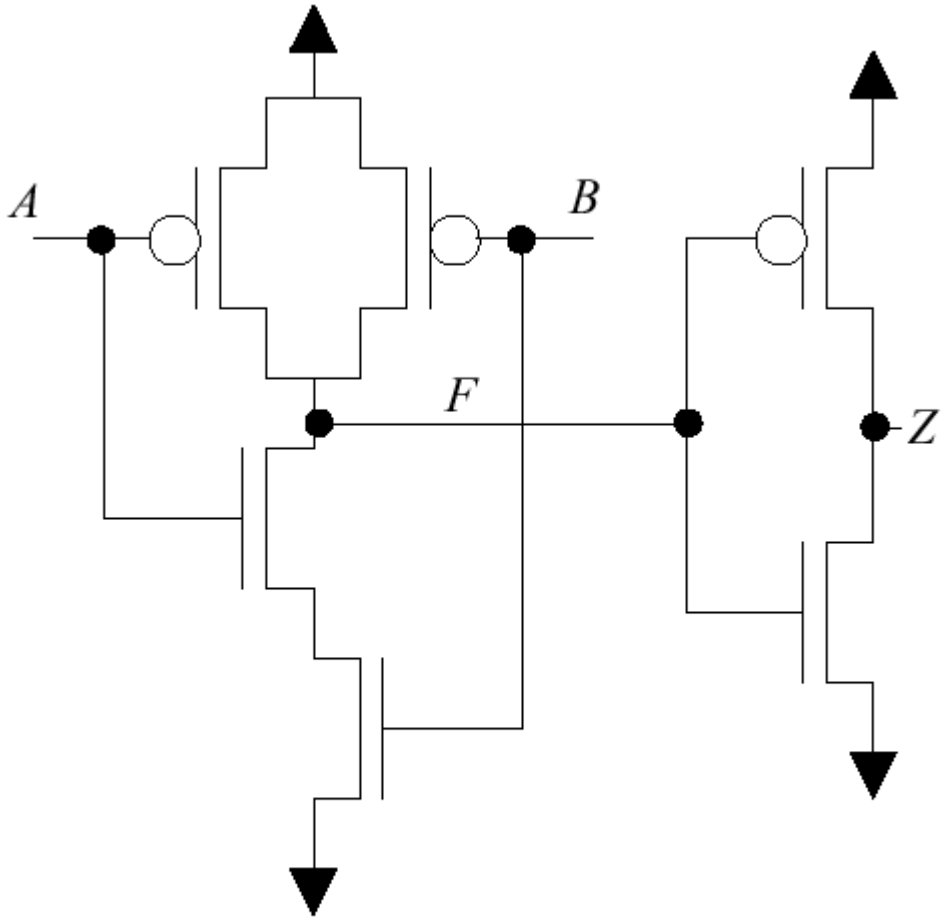

Fig. 4.21 Two-input NAND gate driving an inverter.

RC Model

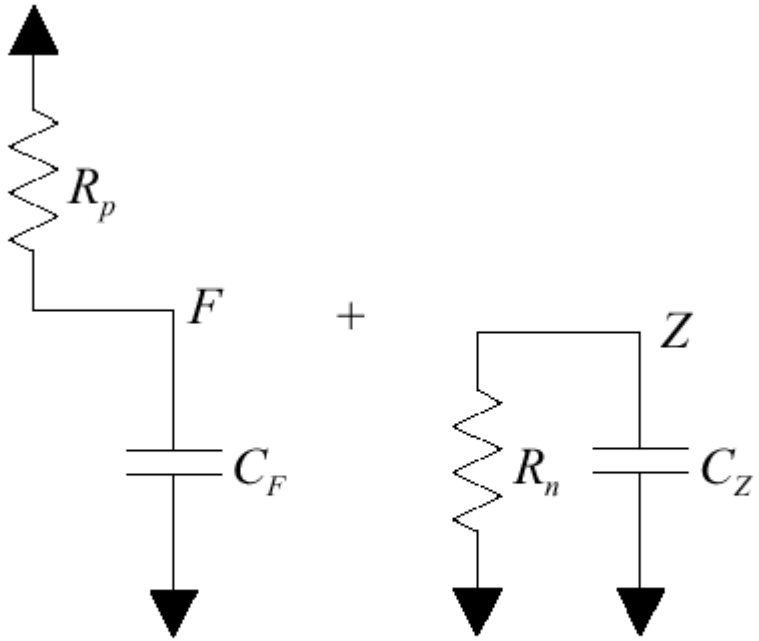

Fig. 4.22 RC model for determining $t_{PHL}(Z)$ and $t_{PLH}(F)$.

RC Model

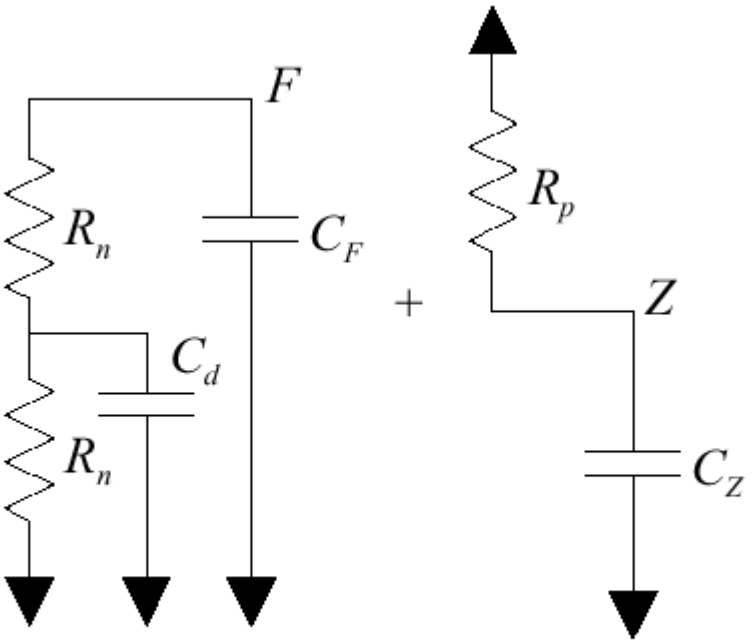

Fig. 4.23 RC model for determining $t_{PHL}(F)$ and $t_{PLH}(Z)$.

Transistor Sizing

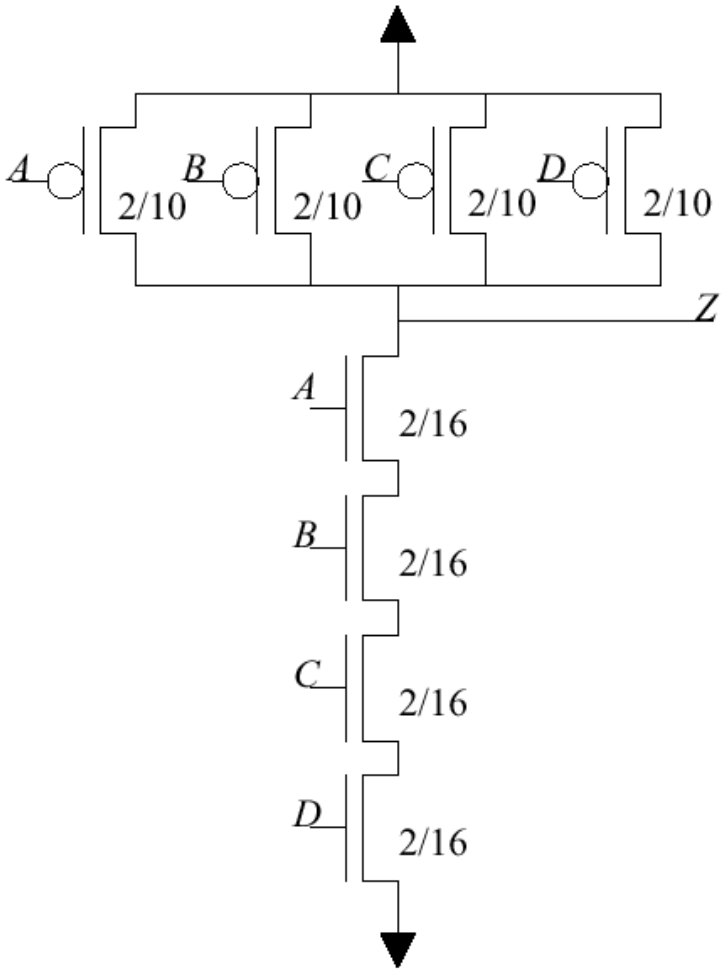

Fig. 4.24 Sizing result of a 4-input NAND gate.

Transistor Sizing

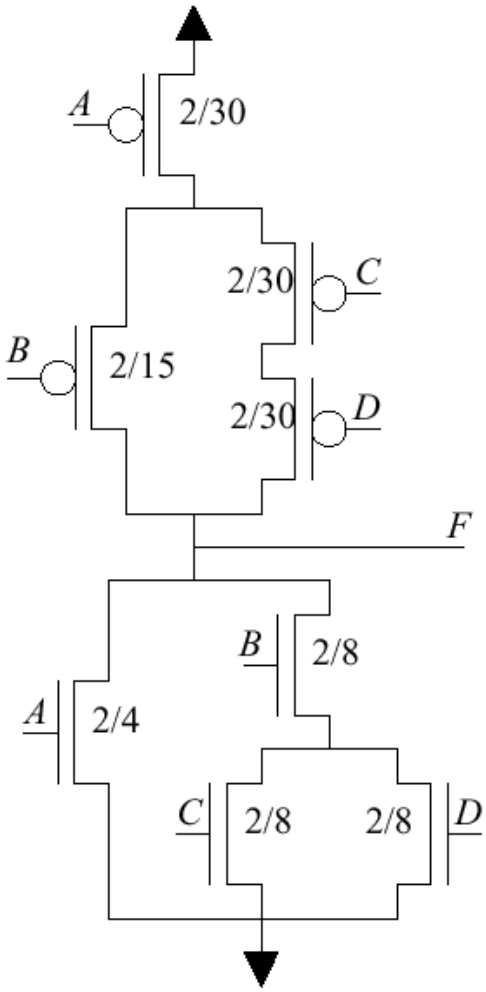

Fig. 4.25 Sizing result of Example 4.5.

Driving Identical Inverter

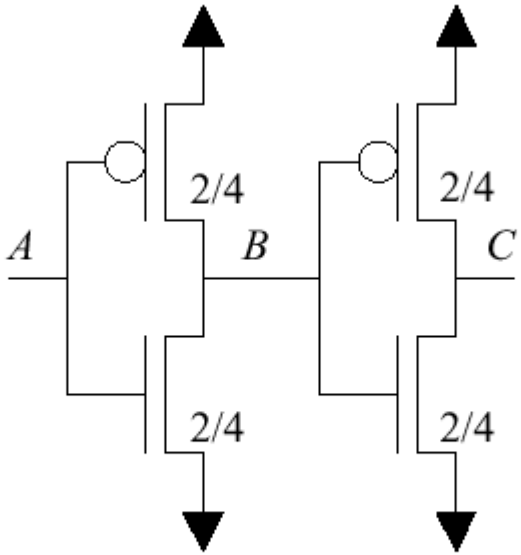

Fig. 4.26 Minimum size inverter driving another identical size inverter.

Driving Identical Inverter

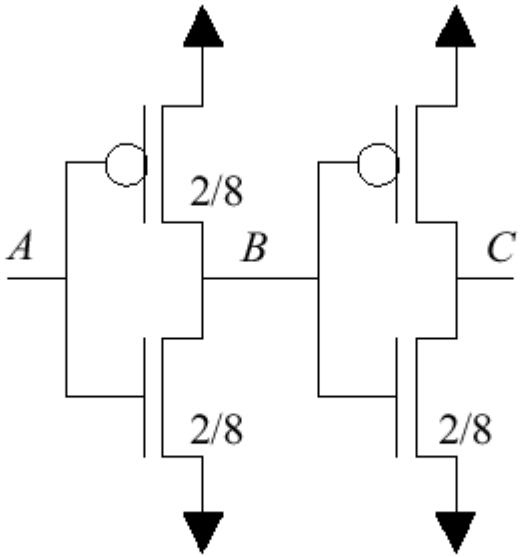

Fig. 4.27 Another example of an inverter driving an identical size inverter.

Driving Identical Inverter

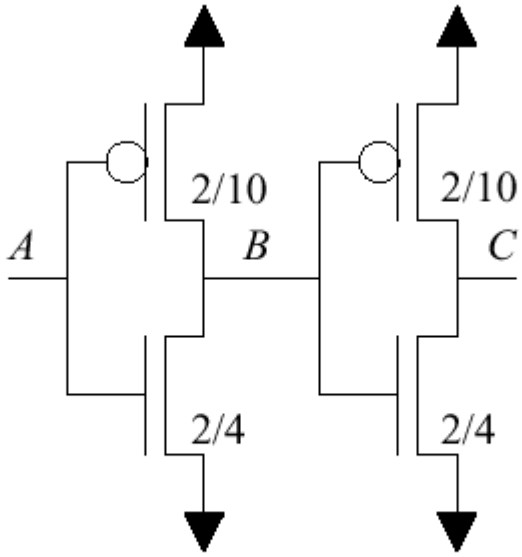

Fig. 4.28 Another example of an inverter driving an identical size inverter.

Buffer

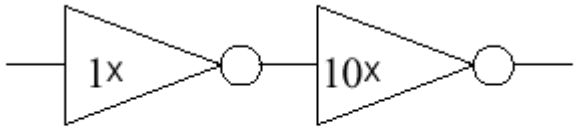

Fig. 4.29 1× inverter driving a 10× inverter.

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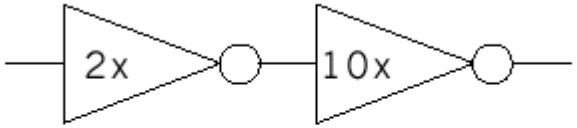

Fig. 4.30 2× inverter driving a 10× inverter.

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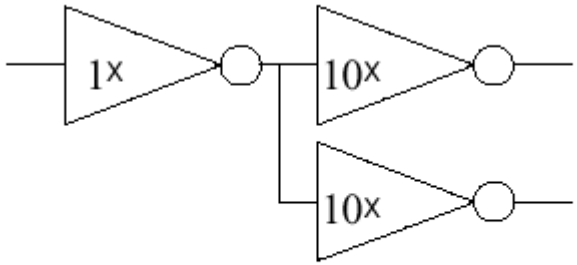

Fig. 4.31 1× inverter driving two 10× inverters.

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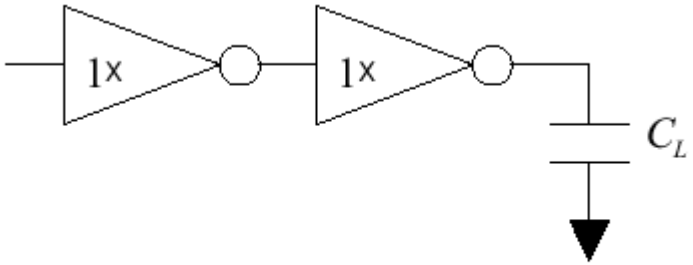

Fig. 4.32 Non-inverting buffer driving a large load.

Buffer

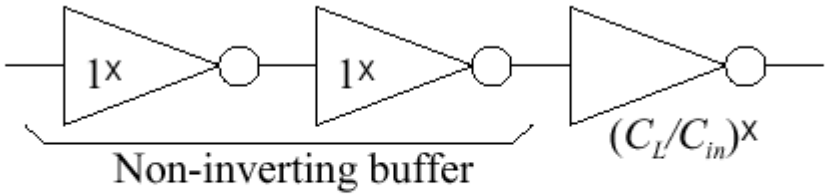

Fig. 4.33 Replacing a large load with a $(C_L/C_{in})\times$ inverter.

Buffer

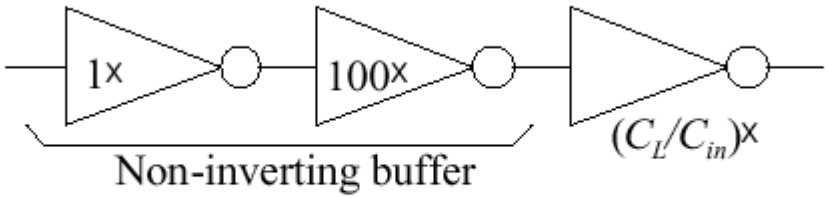

Fig. 4.34 Replacing the second inverter with a 100× inverter.

Driving Large Load

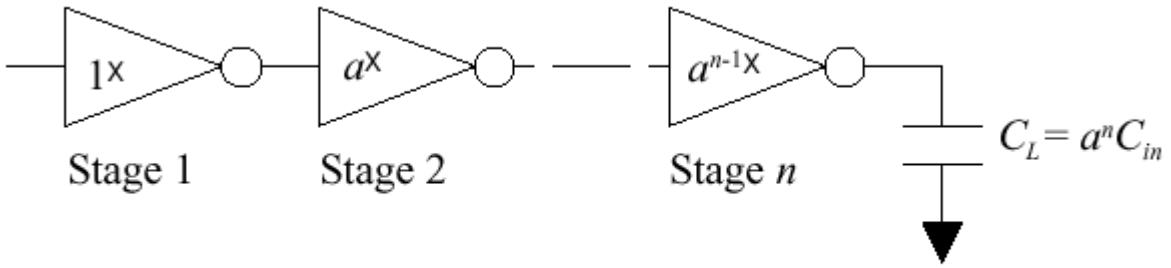

Fig. 4.35 Chain of inverter stages driving a large load.

Charging Load

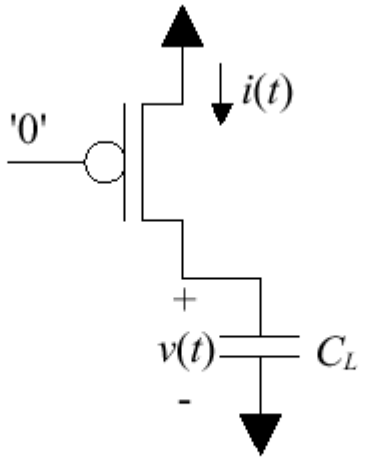

Fig. 4.36 Charging a load capacitance through a pMOS transistor.

Parasitic Bipolar Transistors

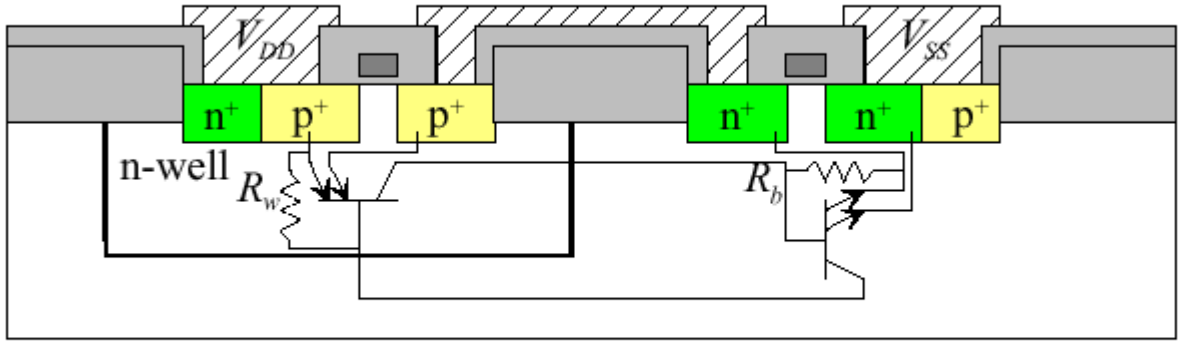

Fig. 4.37 Parasitic bipolar transistors in a CMOS structure.

Parasitic Transistors

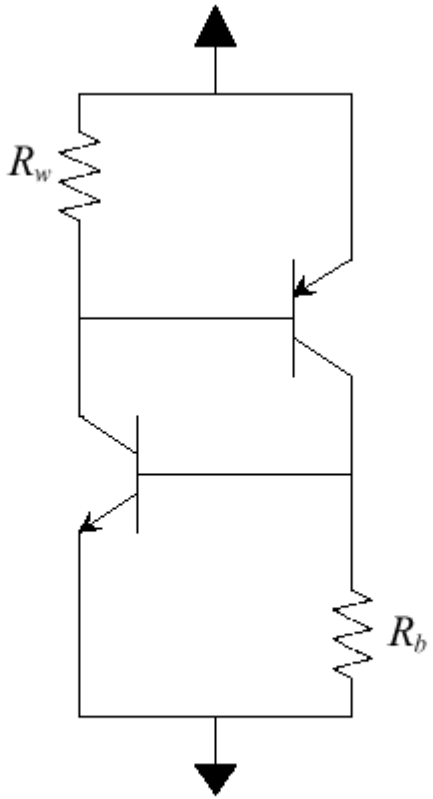

Fig. 4.38 Parasitic transistors of a CMOS logic.